2011 Spintronics Workshop on LSI

Opening Remarks

- Spintronics for Nonvolatile Electronics -

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Supported by the FIRST program of JSPS.

http://www.csis.tohoku.ac.jp/

Challenges

- Static power
- Dynamic power
- Interconnection delay
- Feature size

Making memories

- Nonvolatile
- Small
- Embedded in interconnection
- Part of logic

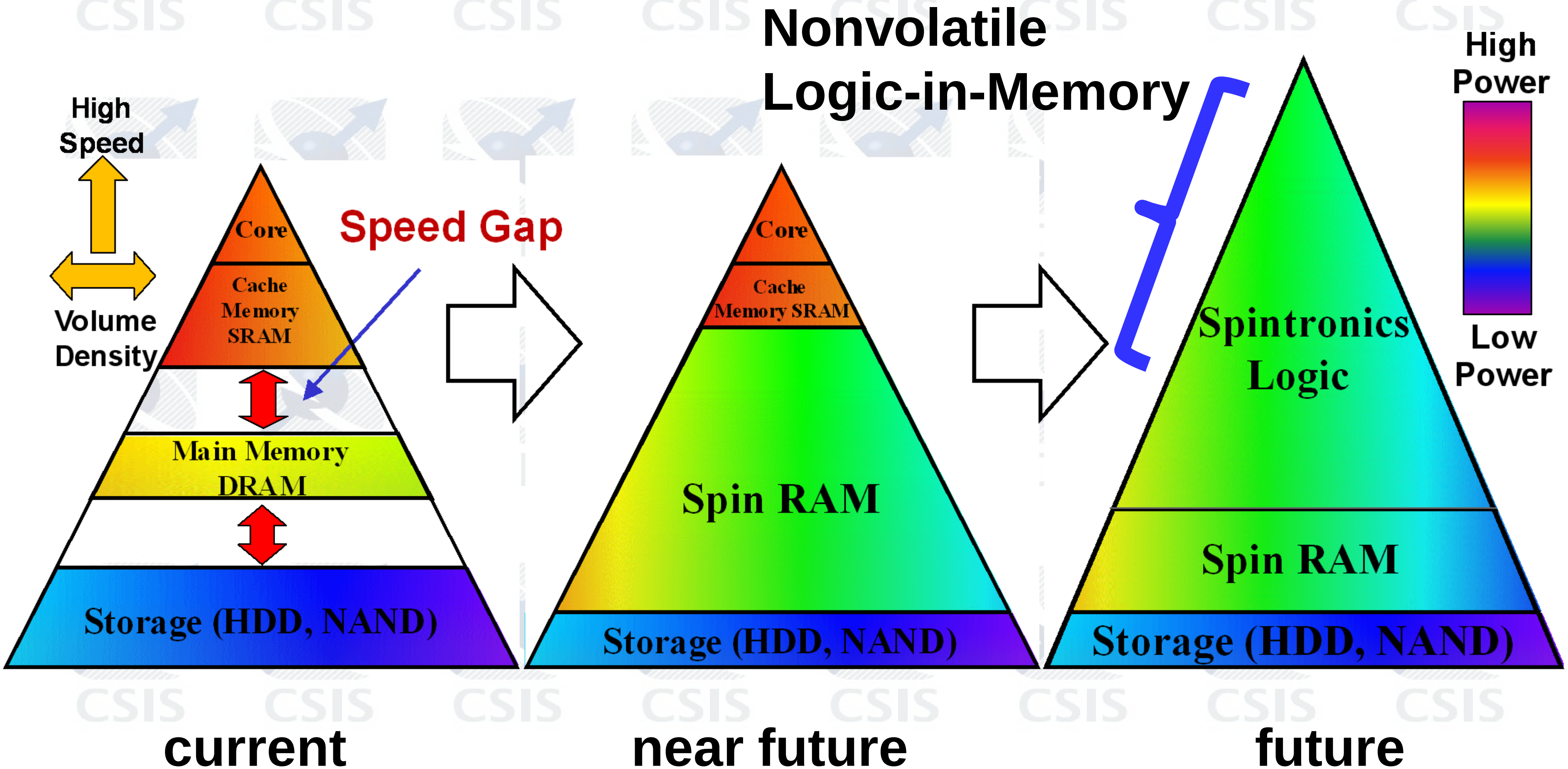
Nonvolatile CMOS Electronics

Comparison of memories

	SRAM	DRAM	Next Generation Nonvolatile Memory				
			PRAM	ReRAM	MRAM	Spin (STT) RAM	FeRAM
Cell Size	～130 F^2	4～8 F^2	4 F^2	4～6 F^2	16～40 F^2	4~ 64F^2	12～25 F^2
High Speed Operation	◎	○	○	○	○	◎	○
Nonvolatility	—	—	○	○	○	○	○
Endurance (limitation of W/E cycle)	◎ (∞)	◎ (∞)	○	○	◎	◎	○
Lower power operation	○	◎	△	△	△	○ ⇒ ◎	◎

T. Endoh, ITRS Emerging Research Memory Technologies Workshop2010
T. Endoh, STS in SEMICON Korea2010 (Invited)

System (Memory) Hierarchy



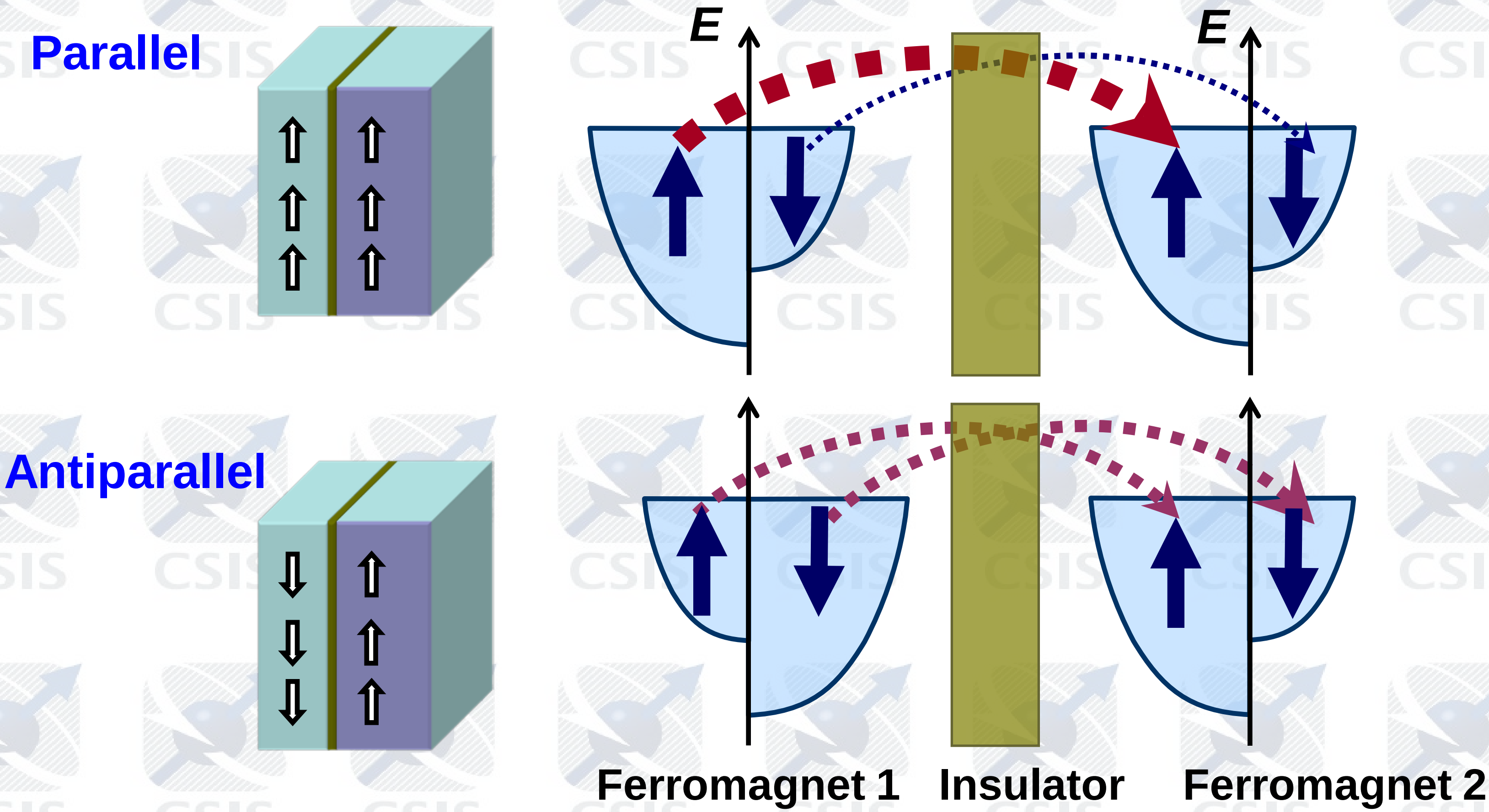
Magnetic tunnel junction based memory elements to counter dynamic and static power, and interconnection delay

Ohno et al. IEDM 2010

Magnetic Tunnel Junction

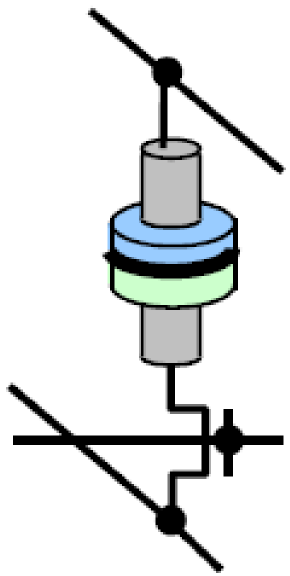
A Spintronics Device

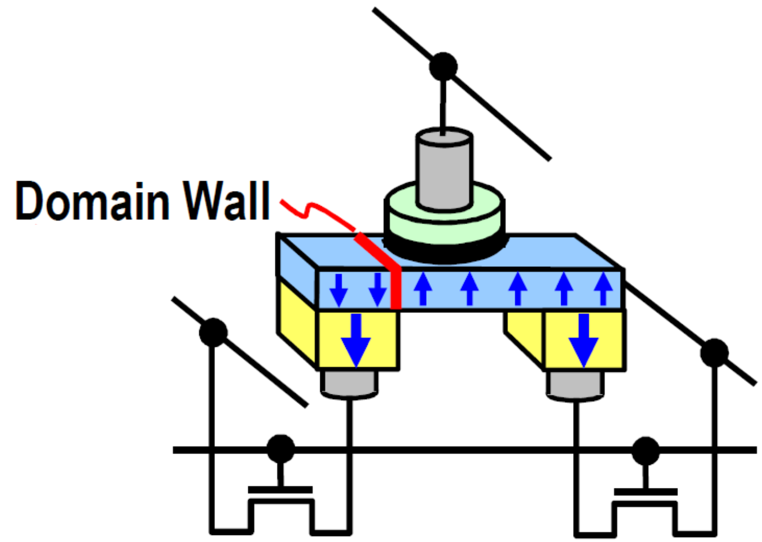
$$\text{Tunnel MagnetoResistance (TMR)} = \frac{R_{AP} - R_P}{R_P} = \frac{2P^2}{1-P^2}$$



Room temperature TMR: Miyazaki and Tezuka (Tohoku U.), *J. Mag. Mag. Mat.* 1995 and Moodera *et al. Phys. Rev. Lett.* 1995.

Magnetic Tunnel Junction Configurations


two terminal



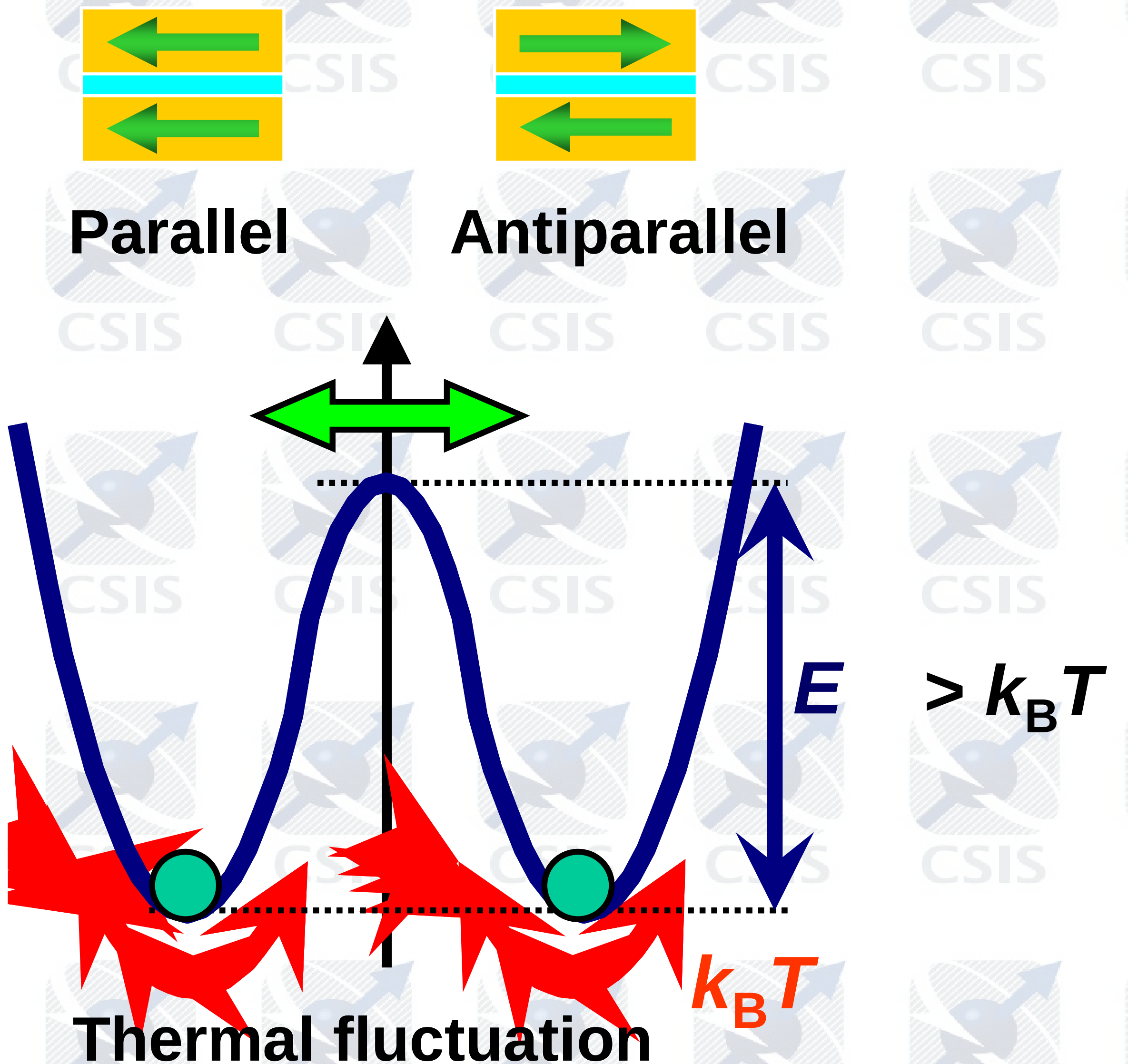
three terminal

nonvolatile, fast and high endurance

MTJ for VLSI: A wish list

1. Small footprint (*F* nm)
2. High output (TMR ratio > 100%)
3. Nonvolatility ($\Delta = E/k_B T > 40$)
4. Low switching current ($I_{C0} < F$ μA)
5. Back-end-of-the-line compatibility (350 ^{o}C)
6. Endurance
7. Fast read & write
8. Low resistance for low voltage operation
9. Low error rate
10. Low cost

I_{c0} and $\Delta = E/k_BT$



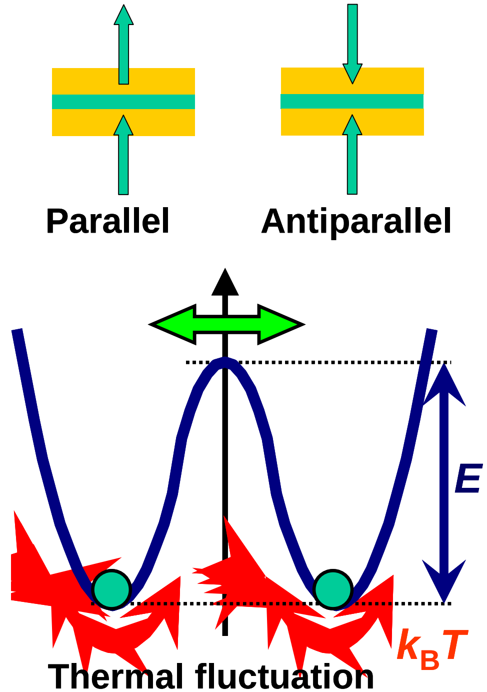
I_{c0} and $\Delta = E/k_B T$

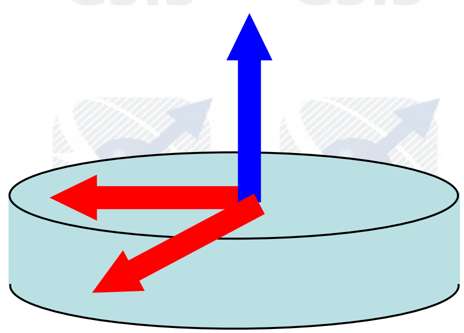
perpendicular

$$E = \left(\frac{1}{2} M_S H_K\right) V = KV$$

$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g}(KV)$$

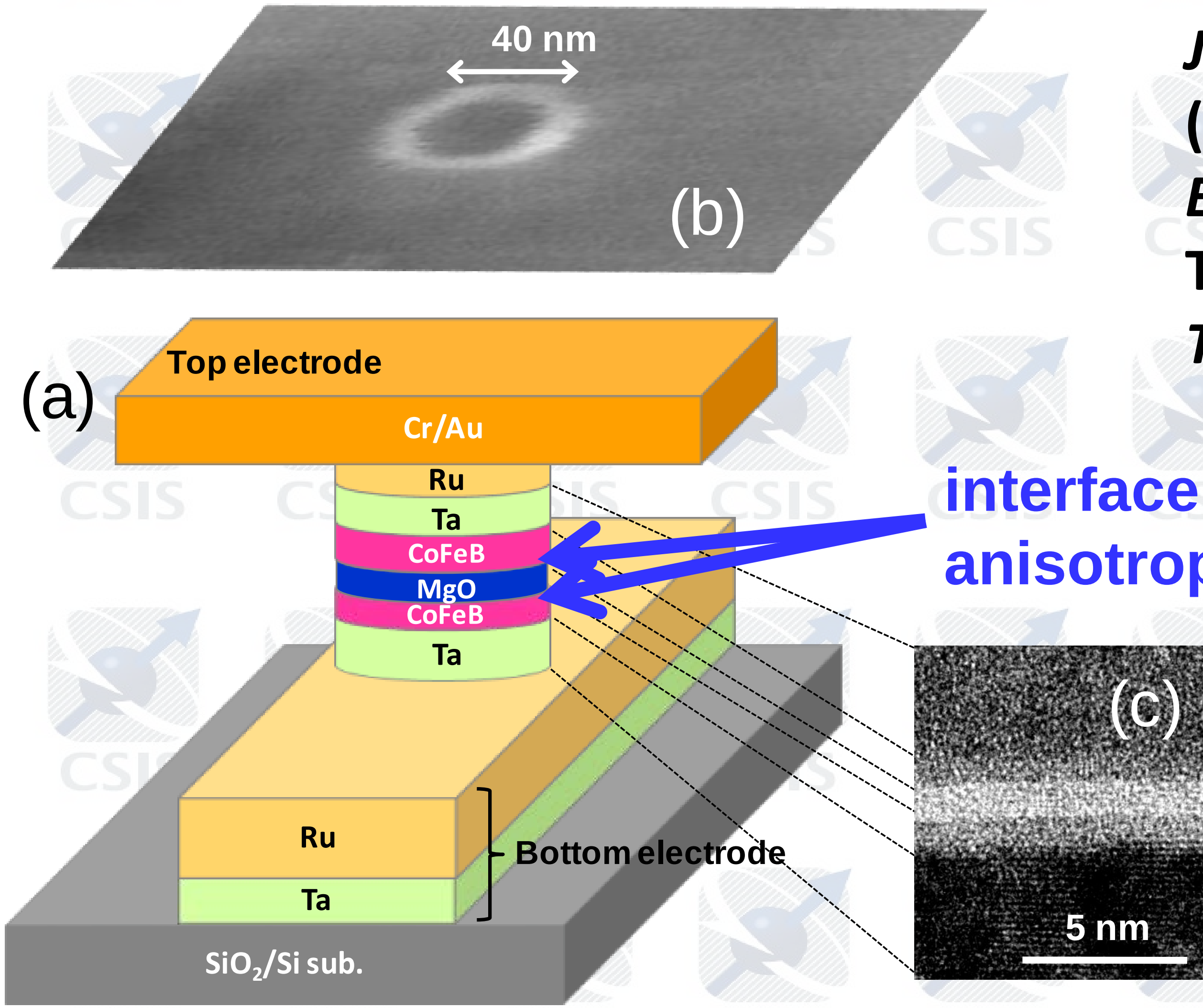
$$\propto \alpha E$$





$$E = \left(K_{shape} + K_{crystalline}\right) V$$

Perpendicular MgO-CoFeB MTJ



J_{C0} = 3.8 MA/cm^2
(I_{C0} = 48 μA)
E/k_BT ~ 40
TMR ratio = 110%
T_a = 350°C

interface perpendicular anisotropy

S. Ikeda et al., Nat. Mat. 9, 721 (2010), K. Miura et al., MMM 2010

Scaling

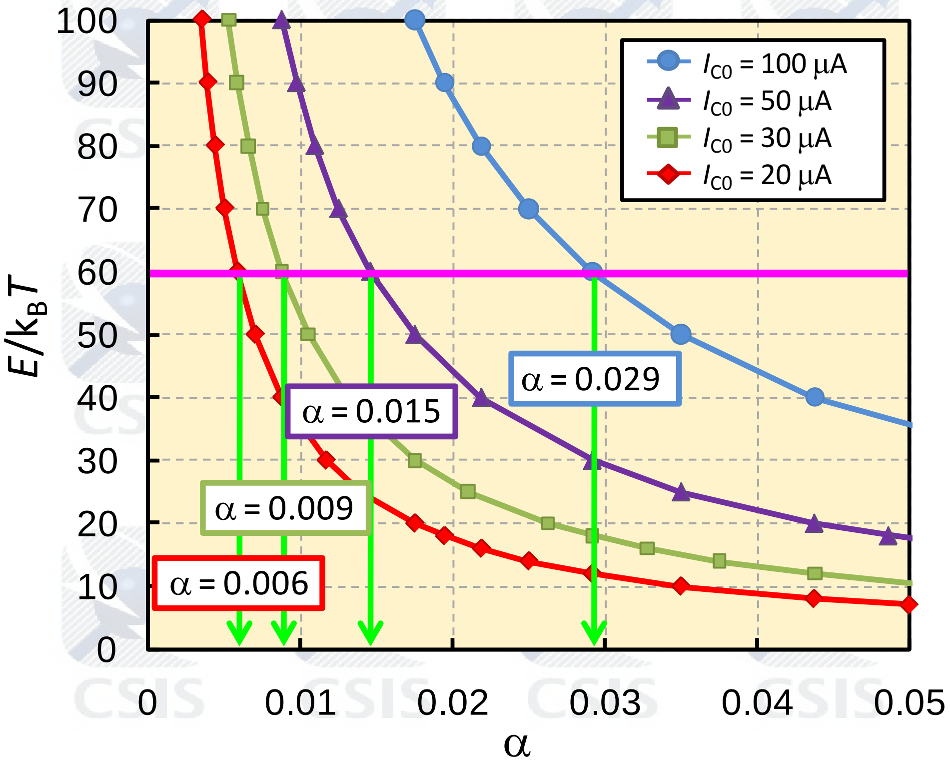
perpendicular

$$E = \left(\frac{1}{2} M_S H_K\right) V = KV$$

$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g}(KV)$$

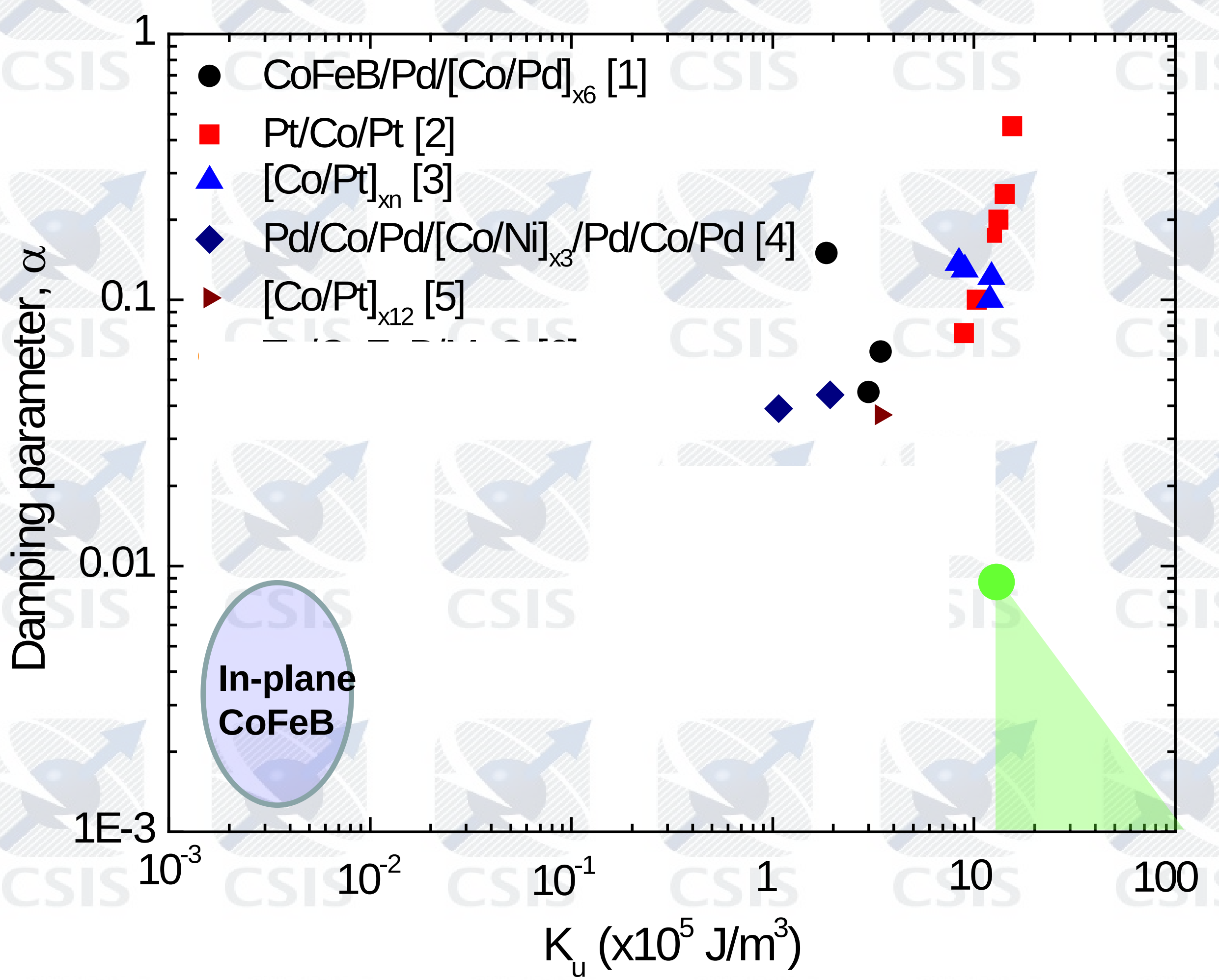
$$\propto \alpha E$$

High $K = \frac{1}{2} M_S H_K$ and low α



$$I_{C0} = 3.4\times10^3 \alpha\,[\mu\text{A}]\ \text{for}\ E = 60 k_B T$$

α versus K_u



Ref. [1] E. P. Sajitha, et. al., IEEE Transactions on Magnetics, **46**, 2056 (2010)

[2] S. Mizukami, et. al., App. Phys. Lett., **96**, 152502 (2010)

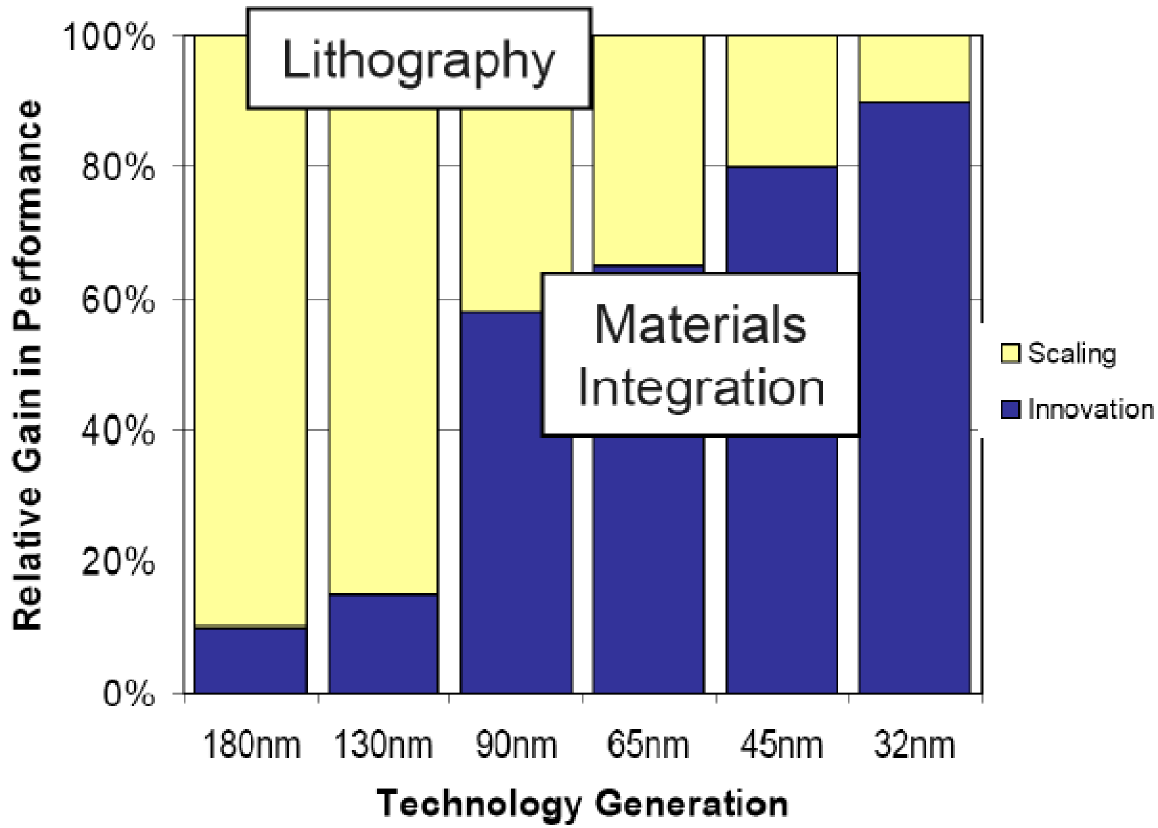
[3] A. Barman, et. al., J. App. Phys., **101**, 09D102 (2007)

[4] J.-M. Beaujour, et. al., Phys. Rev. B., **80**, 180415R (2009)

[5] N. Fujita, et. al., J. Magn. Magn. Mater., **320**, 3019 (2008)

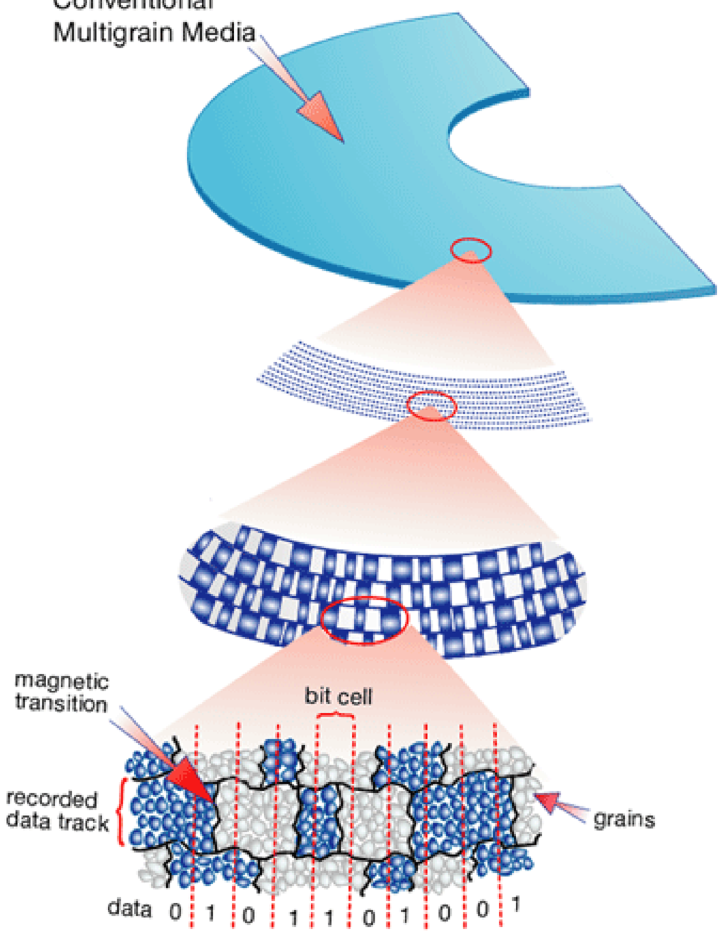
G. Groeseneken
imec – K.U. Leuven

Importance of new materials is growing !

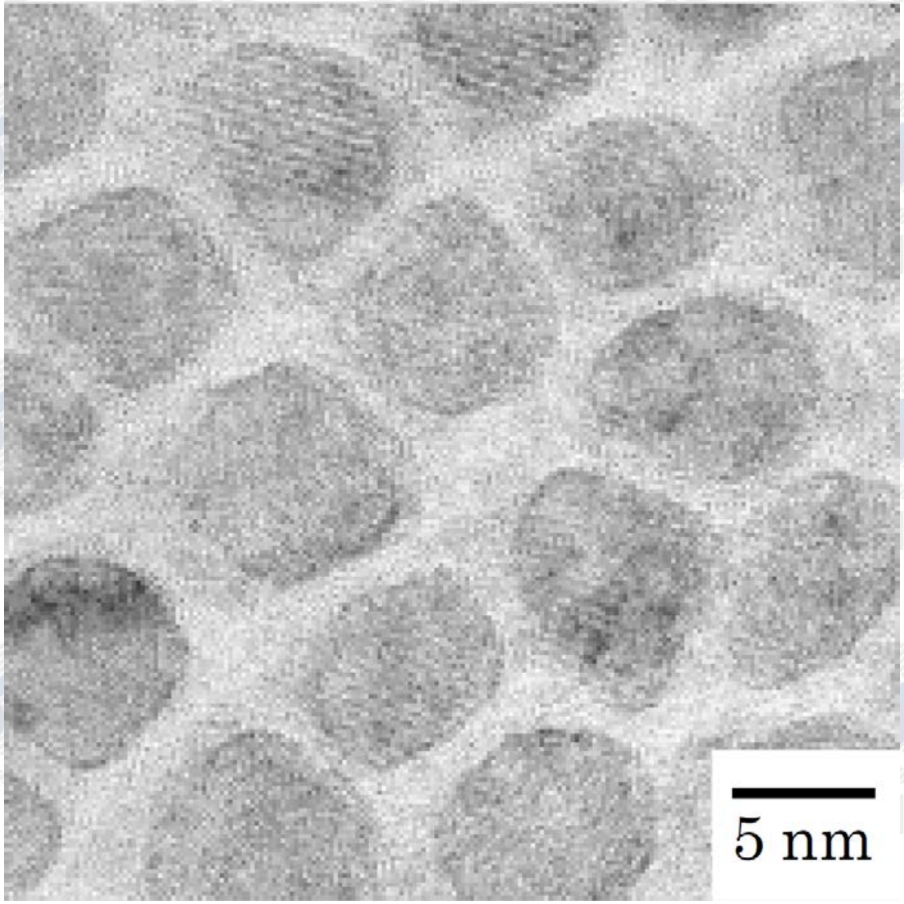


Source – INTEL, IBM

How small can we go?



© Hitachi Global Storage Technologies



CoPtCr-SiO2, Takei *et al.*, Fuji Electric review 55 (2009) 6..

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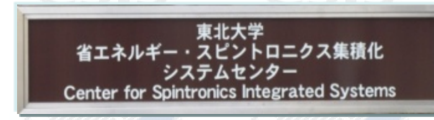

Center for Spintronics Integrated Systems (CSIS)
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Deputy Director：Tetsuo Endoh, Naoki Kasai

- Steering Committee
- Advisory Committee
- Technical Advisory Committee

Support office

Spintronics materials	Shoji Ikeda (Tohoku Univ.)
Spintronics devices	Yasuo Ando (Tohoku Univ.)
New spintronics materials and devices	Fumihiro Matsukura (Tohoku Univ.)
Spintronics processing	Nobuyuki Ishiwata (NEC)
Spintronics logic design and IP development	Takahiro Hanyu (Tohoku Univ.)
Design tool development for spintronics VLSI	Tetsuo Endoh (Tohoku Univ.)
Spintronics VLSI demonstration	Tadahiko Sugibayashi (NEC)

- Tsukuba site : Tsukuba Innovation Arena (TIA)
- Participating organization :Tohoku University, NEC, Hitachi, ULVAC, National Institute of Material Science, University of Tokyo
- Collaborating organization : AIST, JST

PROGRAM

Room : Suzaku II (Kibune) 2F	
Opening 7:30 pm - 7:50 pm	**Opening Remarks: Spintronics for Nonvolatile Electronics** Hideo Ohno (Tohoku University, Workshop Chair)
Invited talk 7:50 pm - 8:15 pm	**Recent Progress and Emerging Technology of Spintronics Device for VLSI** Jean-Pierre Nozieres (Spintec)
Invited talk 8:15 pm - 8:40 pm	**Challenges in Non-volatile Etch** Joydeep Guha (Lam Research)
Invited talk 8:40 pm - 9:05 pm	**Technology, Manufacturing and Markets of Magnetoresistive Random Access Memory (MRAM)** Brad Engel (Everspin Technologies)
Invited talk 9:05 pm - 9:30 pm	**Advances in Materials and Structures for STT-RAM** Vladimir Nikitin (Grandis)
Invited talk 9:30 pm - 9:55 pm	**Embedded Spintronics Integrated Circuits for System-on-Chips** Seung Kang (Qualcomm)
Invited talk 9:55 pm - 10:20 pm	**MTJ-Based Nonvolatile Logic-in-Memory Architecture** Takahiro Hanyu (Tohoku University)

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