

A Content Addressable Memory Using Magnetic Domain Wall Motion Cells

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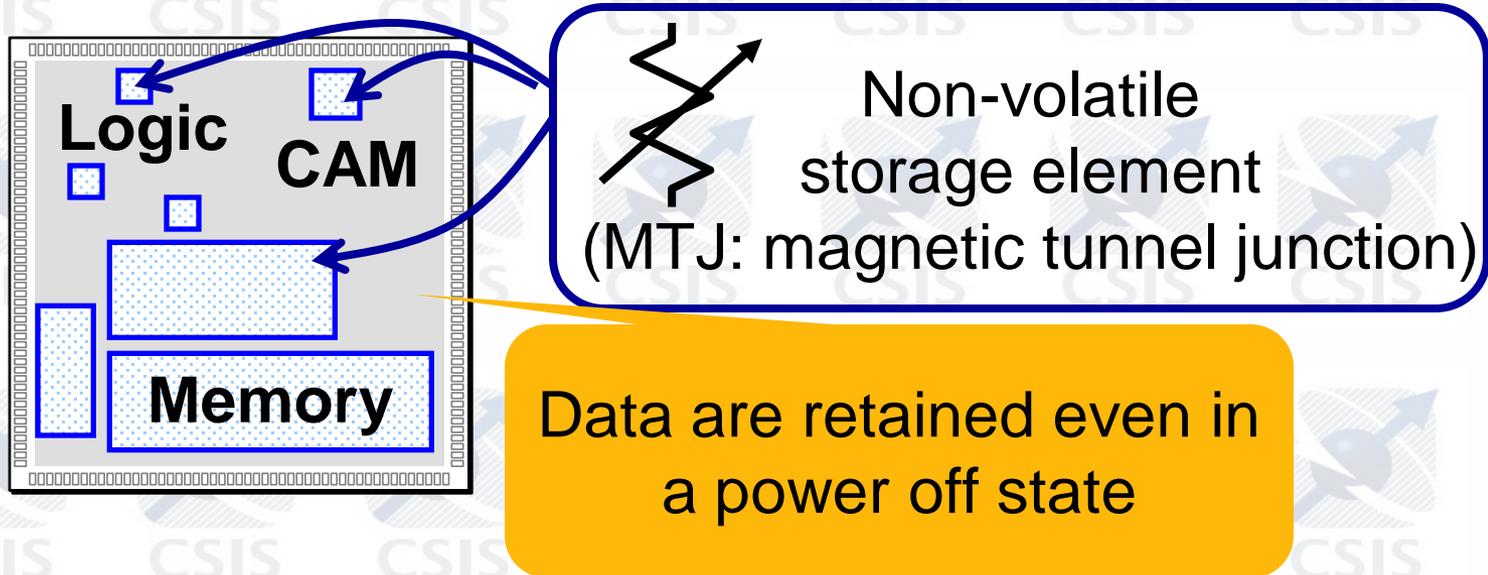
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² Tohoku University, Japan

Outline

- Introduction
- Demonstration of Spintronics-based CAM Test Chip
 - Multi-free layer domain wall (DW) motion cell
 - Shared write transistor
- Future Challenge
 - Multi-context Spin CAM
 - Domain wall motion in CoFeB
- Summary

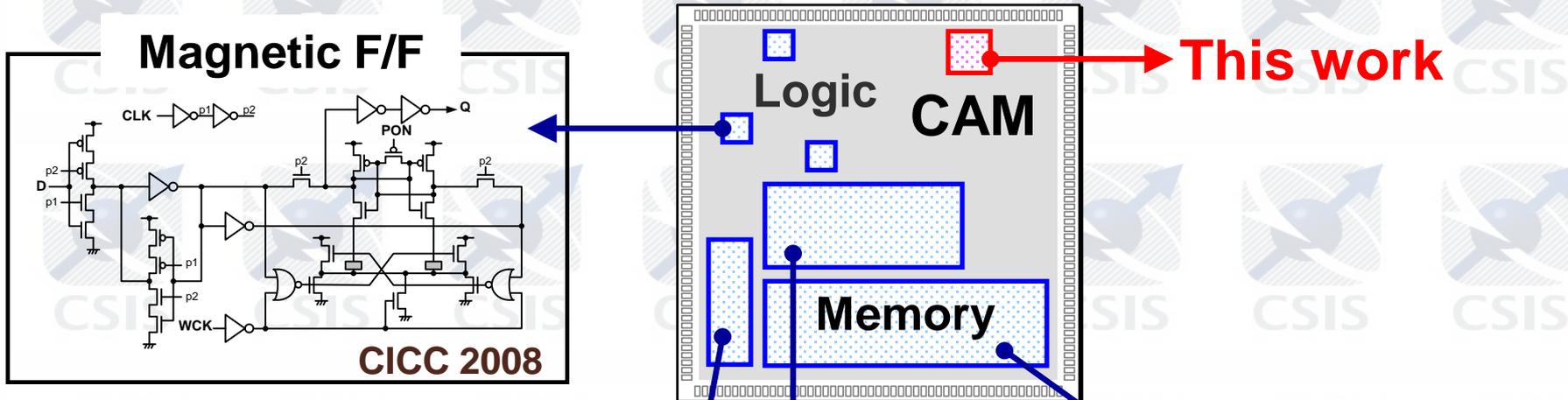
Motivation



Non-volatile Spintronics SoC with power gating

- Reduced leakage current
- Small power penalty for state retention and reload

Overview of Spintronics Core on SoC

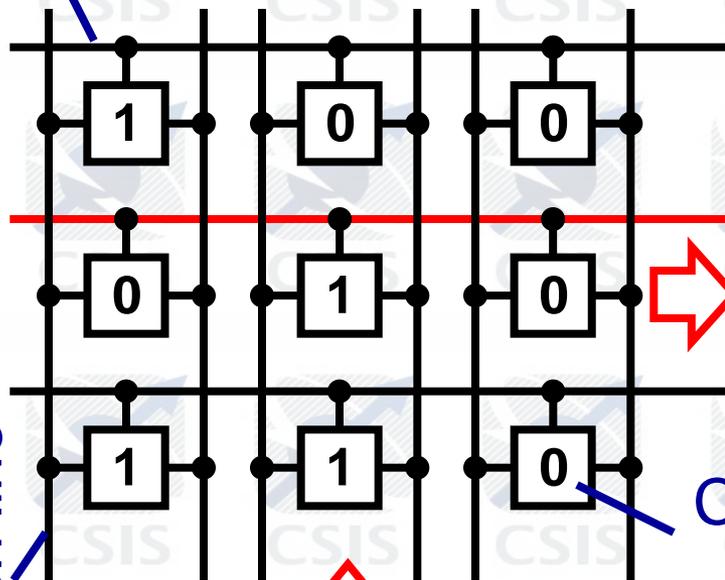


Speed	~ 500 MHz	~ 200 MHz	~ 33 MHz
Capacity	Small	Medium	Large
Cell	<p>5T2MTJ</p> <p>VLSI Cir. 2006</p>	<p>2T1MTJ</p> <p>VLSI Cir. 2006</p>	<p>9T8MTJ/8bit</p> <p>A-SSCC 2007</p>

- Different MTJ cell is needed for different layer in memory hierarchy
- However, the best MTJ cell for CAM is not existed

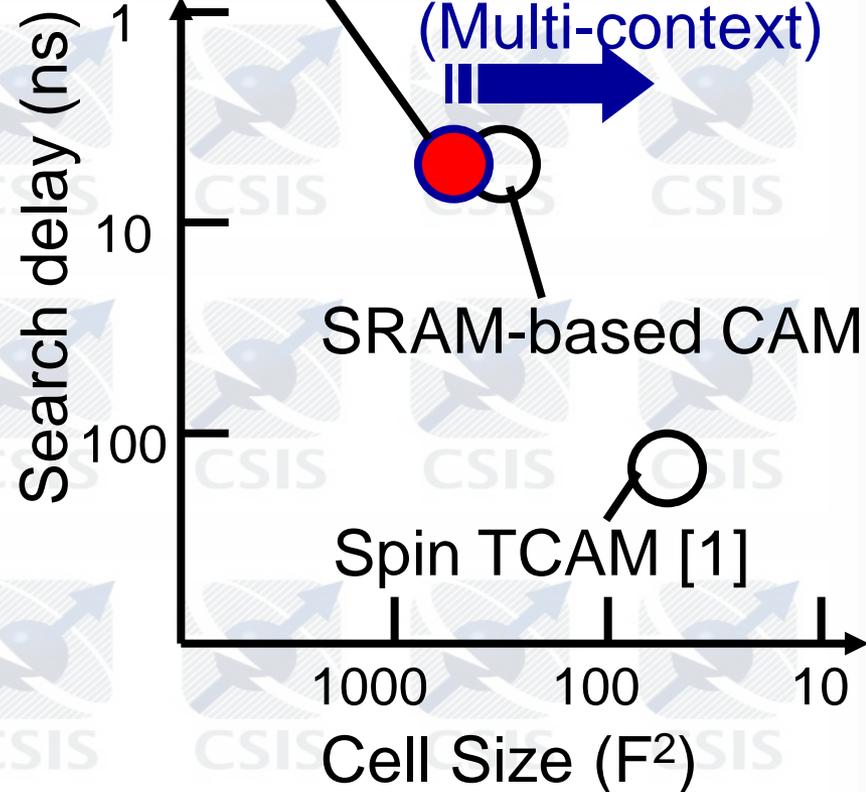
Content Addressable Memory (CAM)

Match line



Non-volatile test chip

in this work Future challenge (Multi-context)



Search line

Match location

CAM cell

Search Data { 0, 1, 0 }

Design target

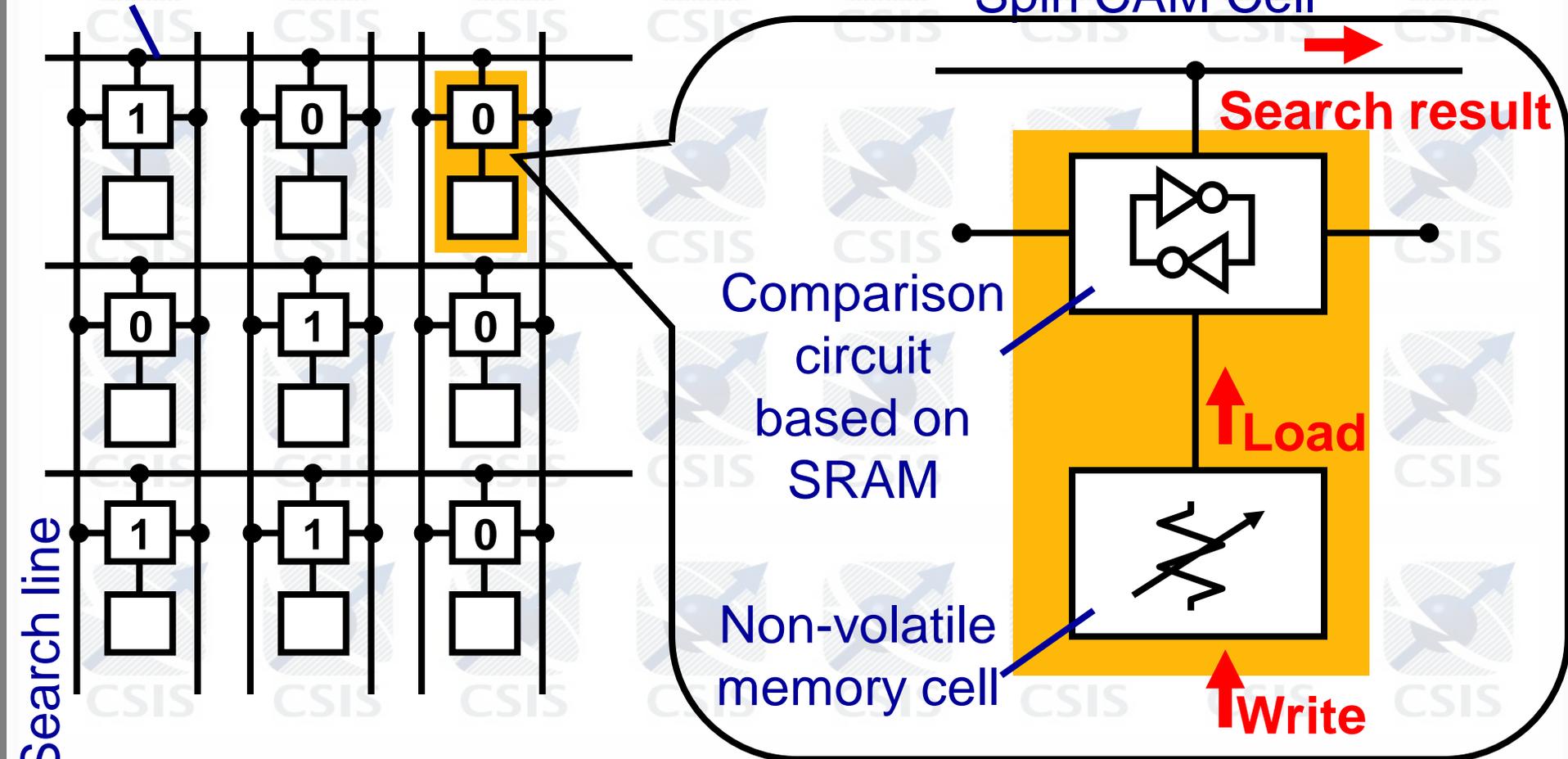
Fast search and Compact

[1] S. Matsunaga et al., APEX, 2, 023004, 2009.

Basic Concept of Spin CAM

Match line

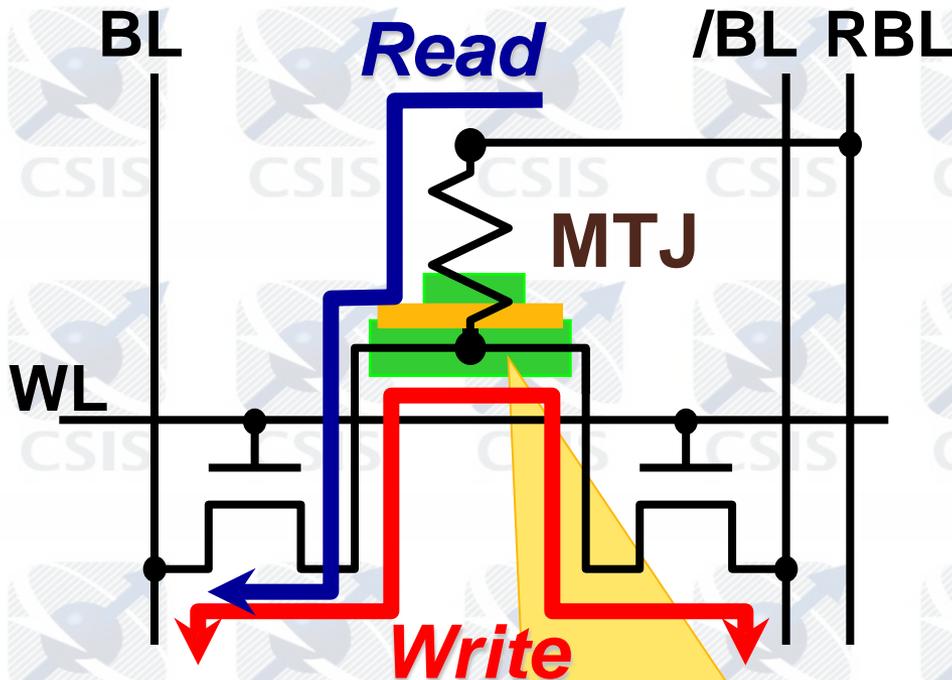
Spin CAM Cell



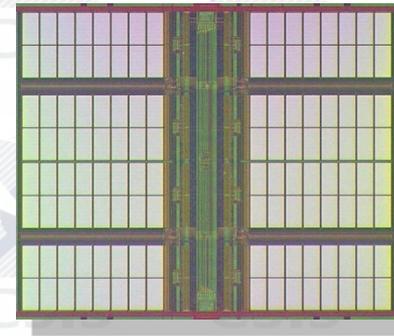
- Once data are transferred from non-volatile memory to comparison circuit, fast search is executable

2Tr-1MTJ Cell for High Speed R/W Operation

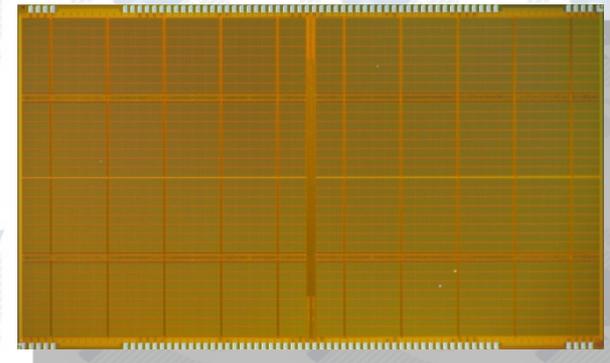
2Tr-1MTJ cell



3-terminal magnetic element



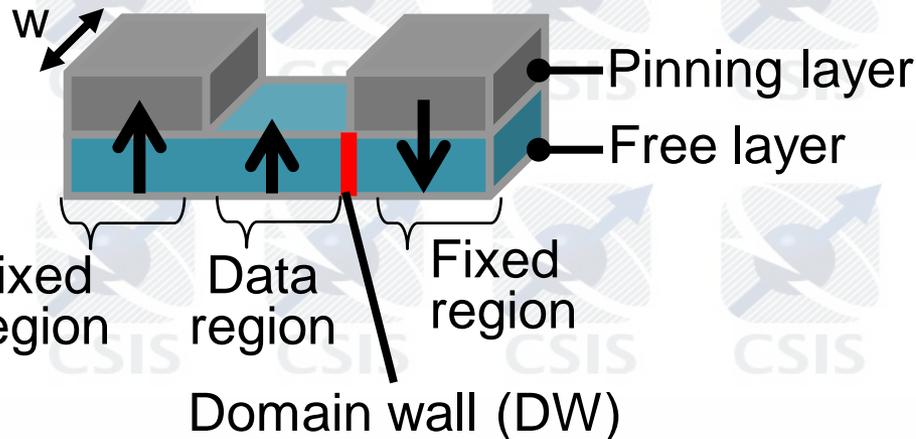
250MHz (ASSCC 2007)



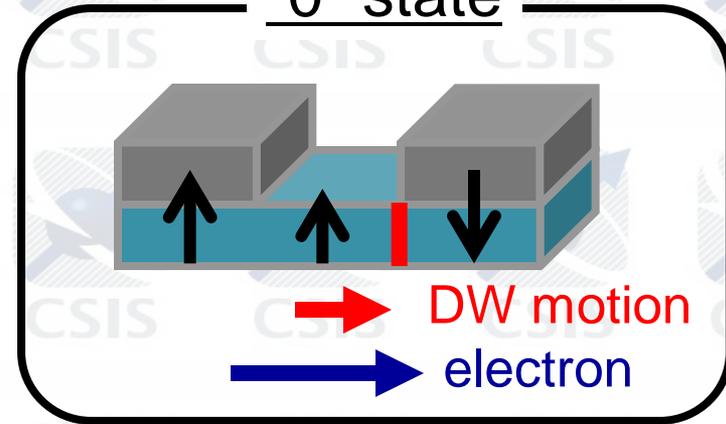
32Mbit (ISSCC 2009)

- High speed operations were demonstrated by using 3-terminal element with magnetic field writing.

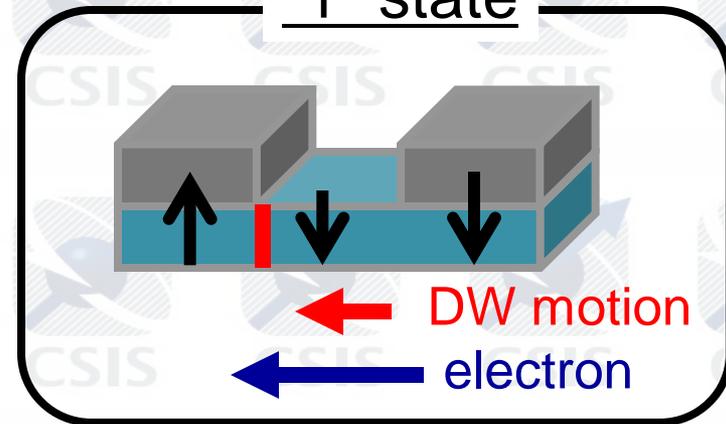
Magnetic Domain Wall Motion Cell



"0" state



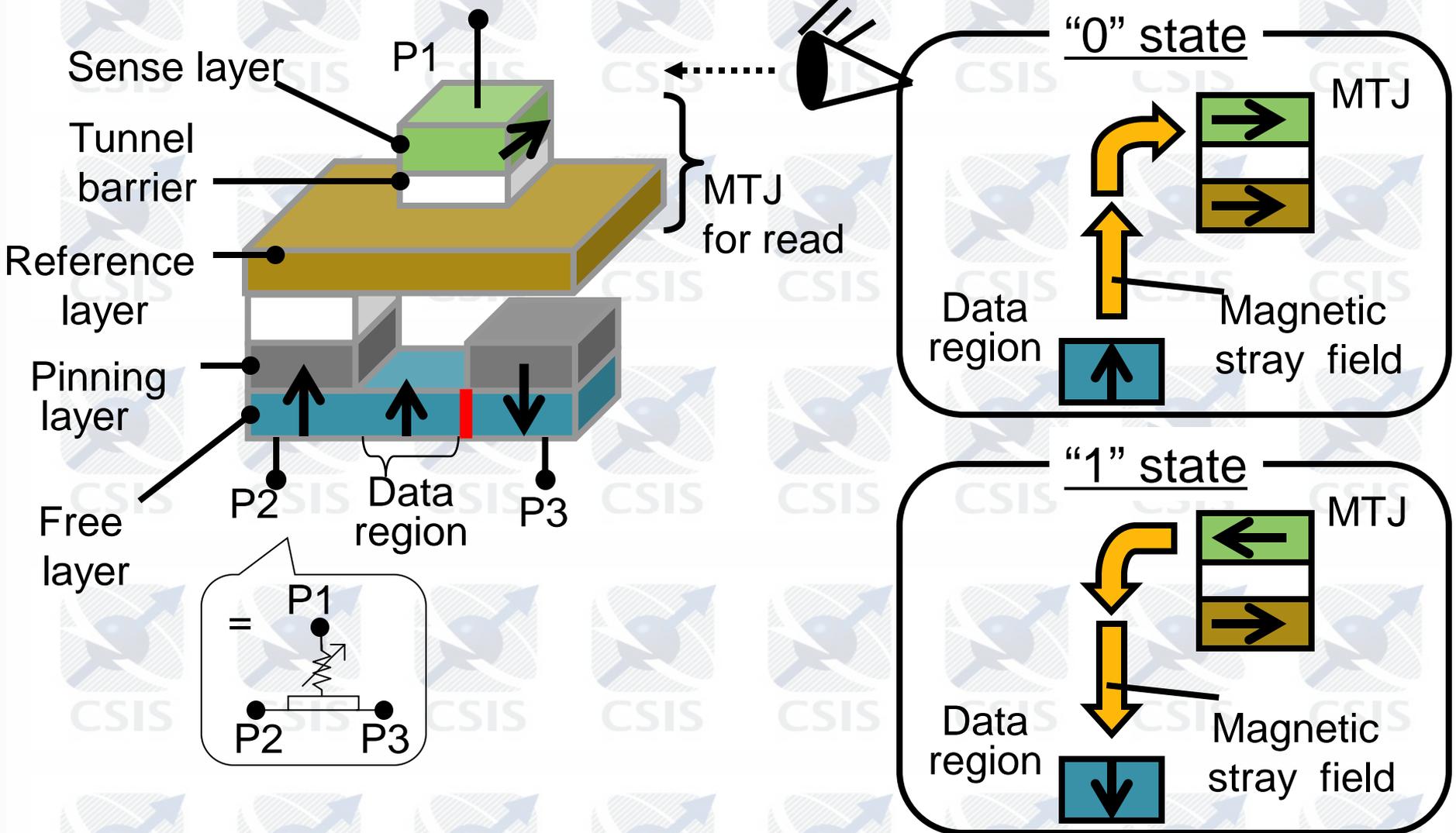
"1" state



VLSI 2009

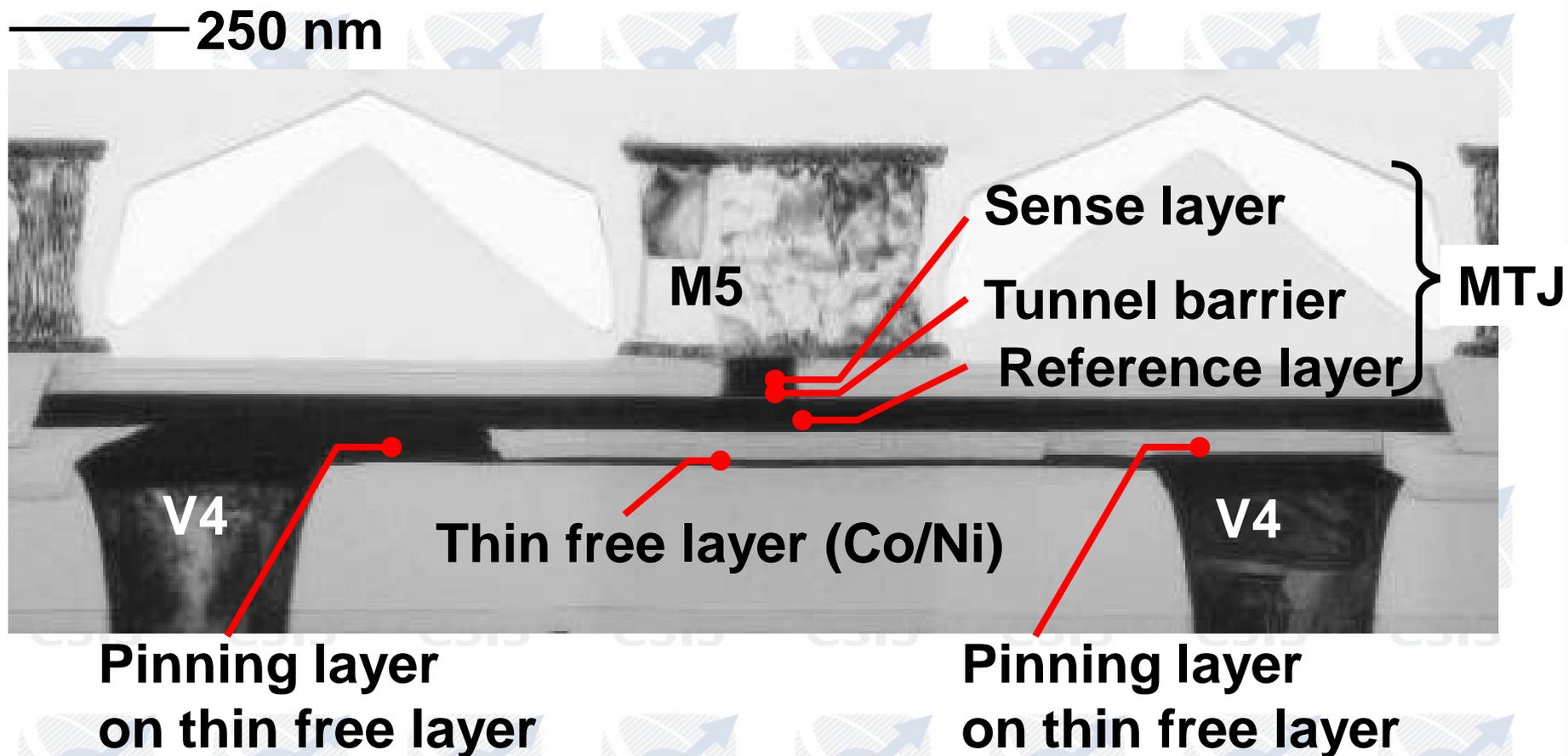
- Low writing current ($200 \mu\text{A}$ @ $w = 90 \text{ nm}$) was obtained

Multi-free Layer Domain Wall Motion Cell

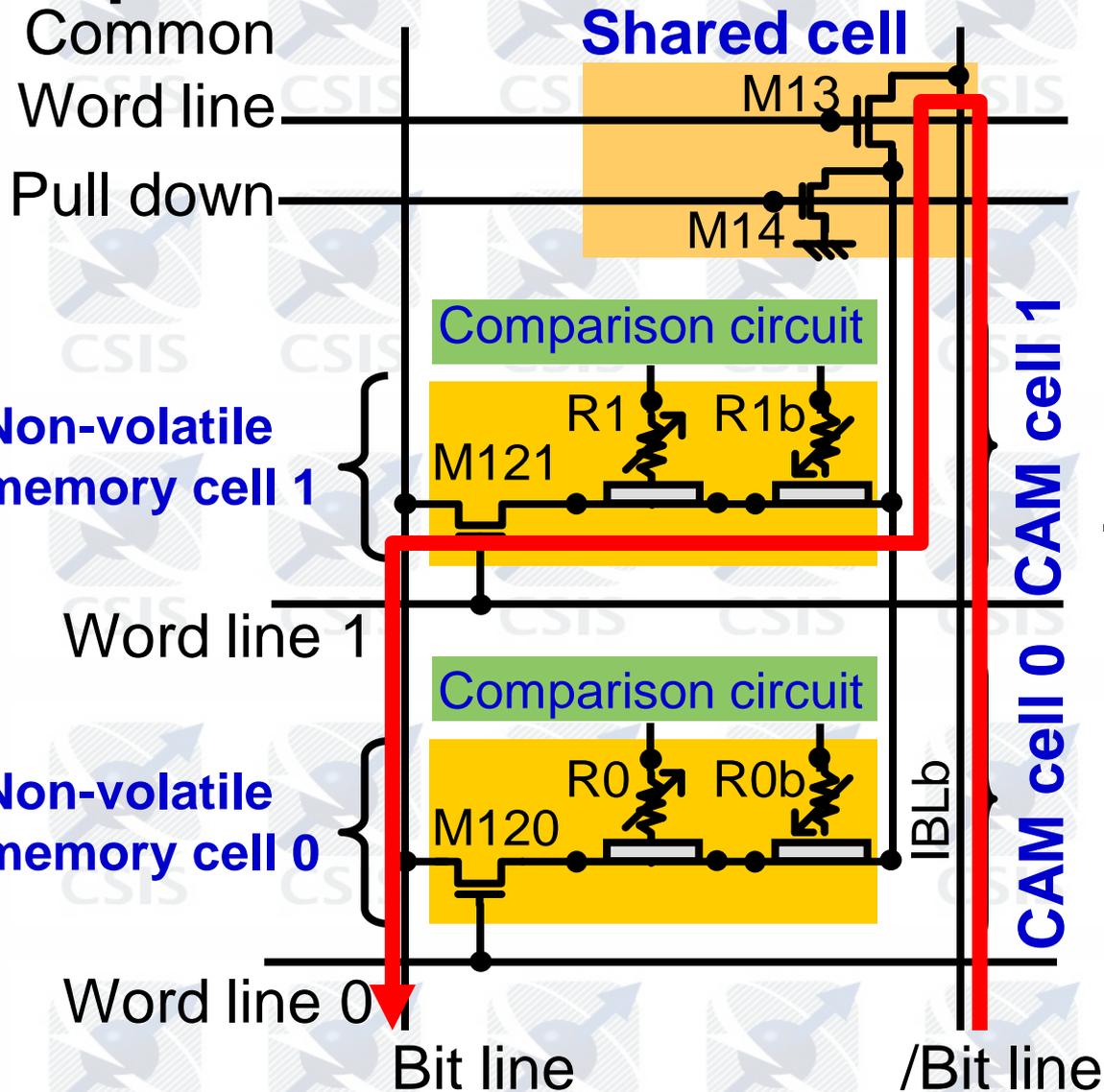


- Fast read operation and low writing current were obtained

Multi-free layer Domain Wall Motion Cell



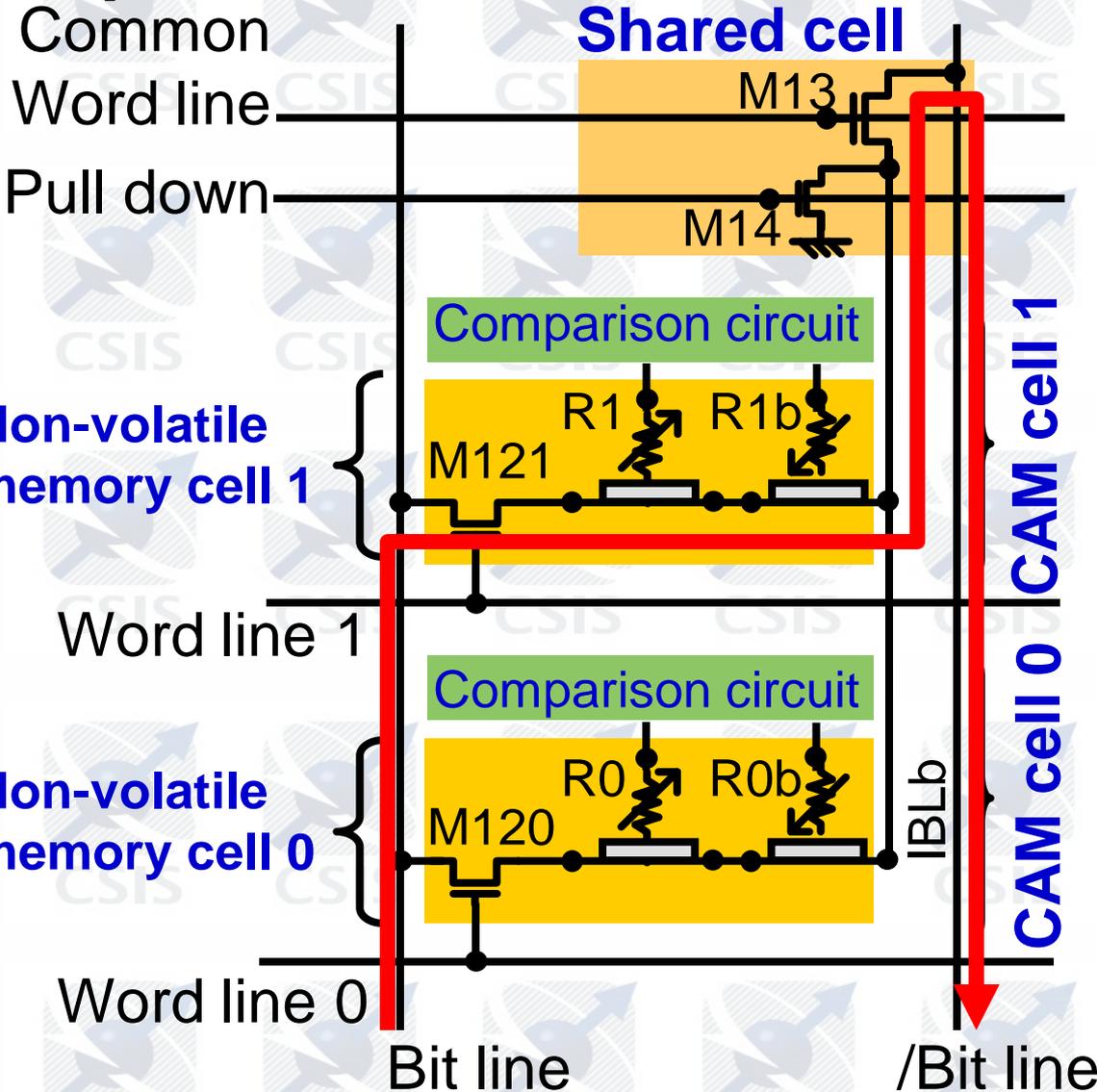
Spin CAM with Shared Write Transistor



- 3-terminal elements (R_1 and R_{1b}) share write transistor (M_{13} , M_{121})
- CAM cells share write transistor (M_{13})
- Cell area reduced

Write current $I_w(0)$

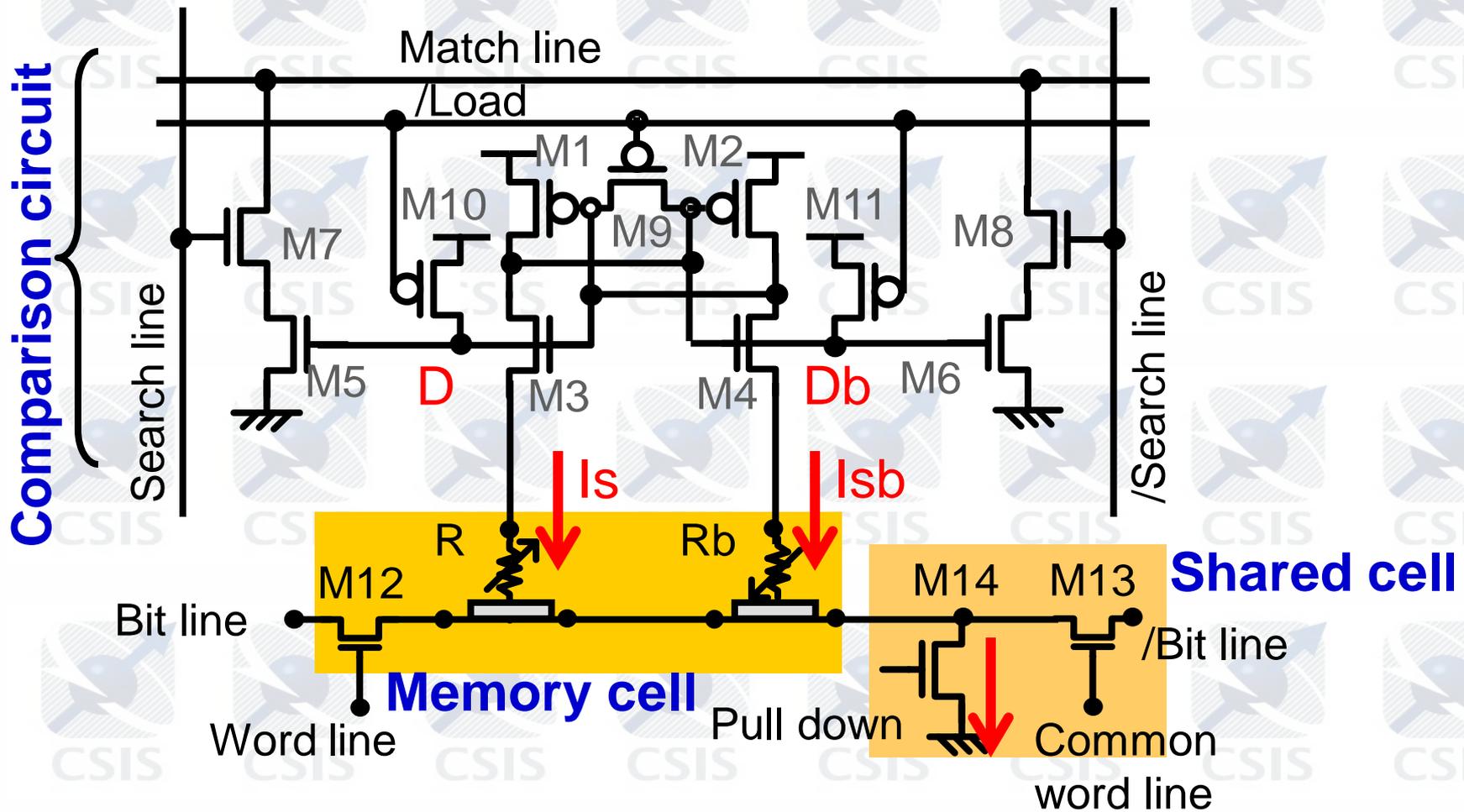
Spin CAM with Shared Write Transistor



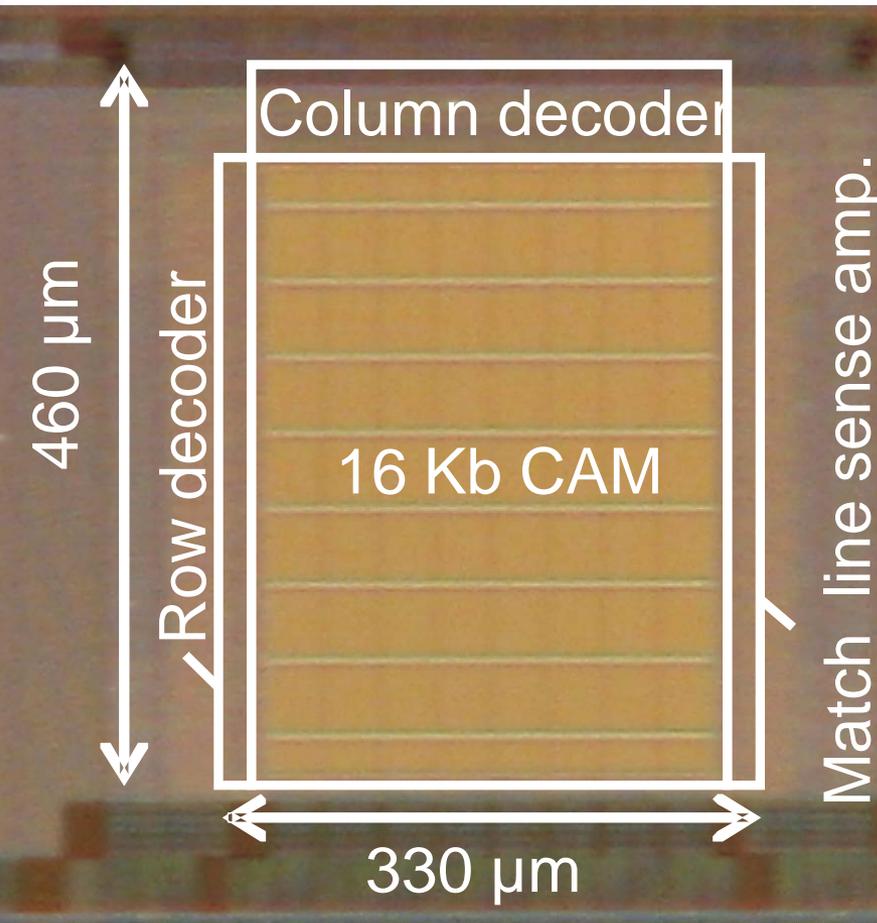
- 3-terminal elements (R1 and R1b) share write transistor (M13, M121)
- CAM cells share write transistor (M13)
- Cell area reduced

Write current I_w (1)

Load Operation of Spin CAM

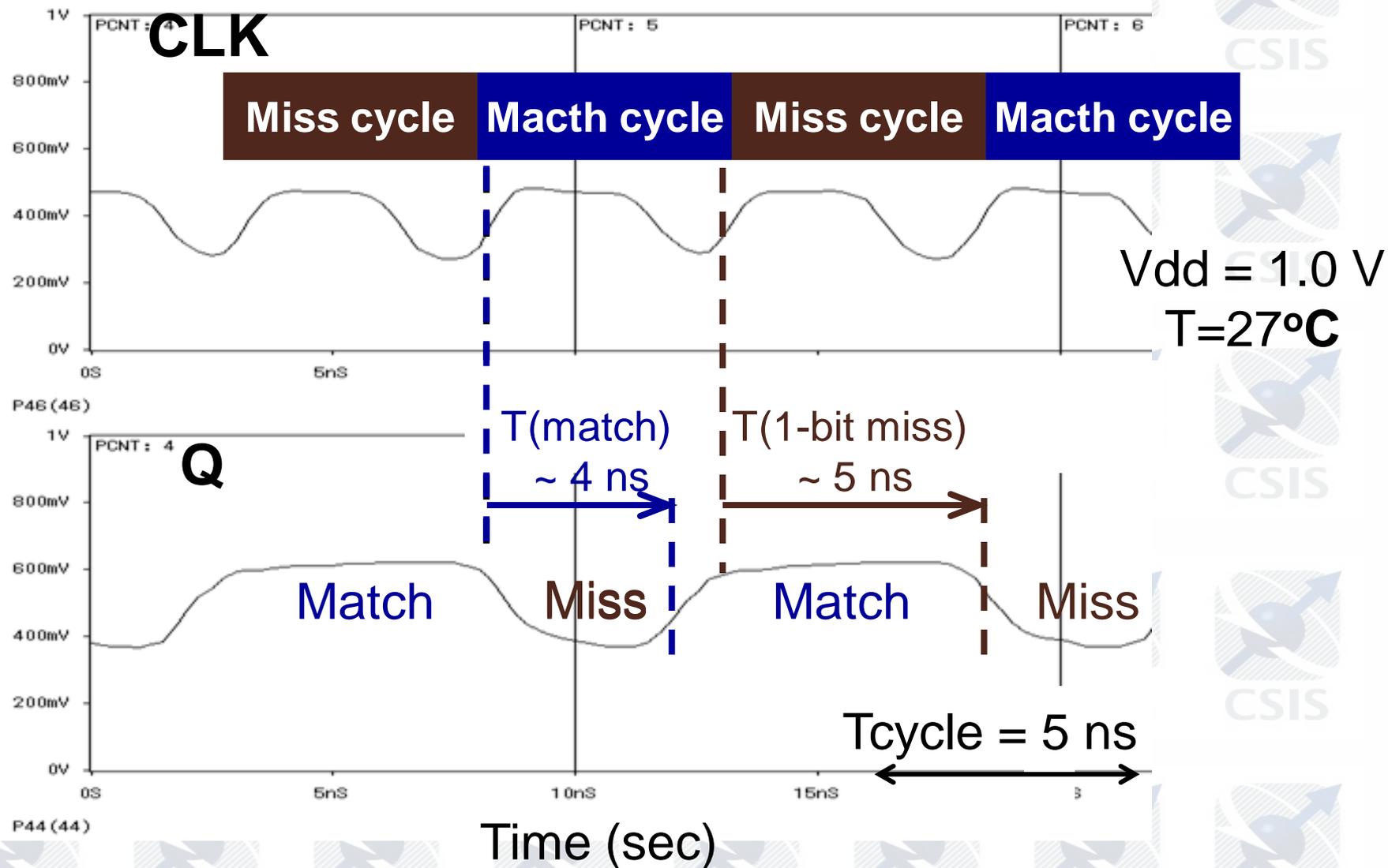


16-Kbit Spin-CAM Test Chip

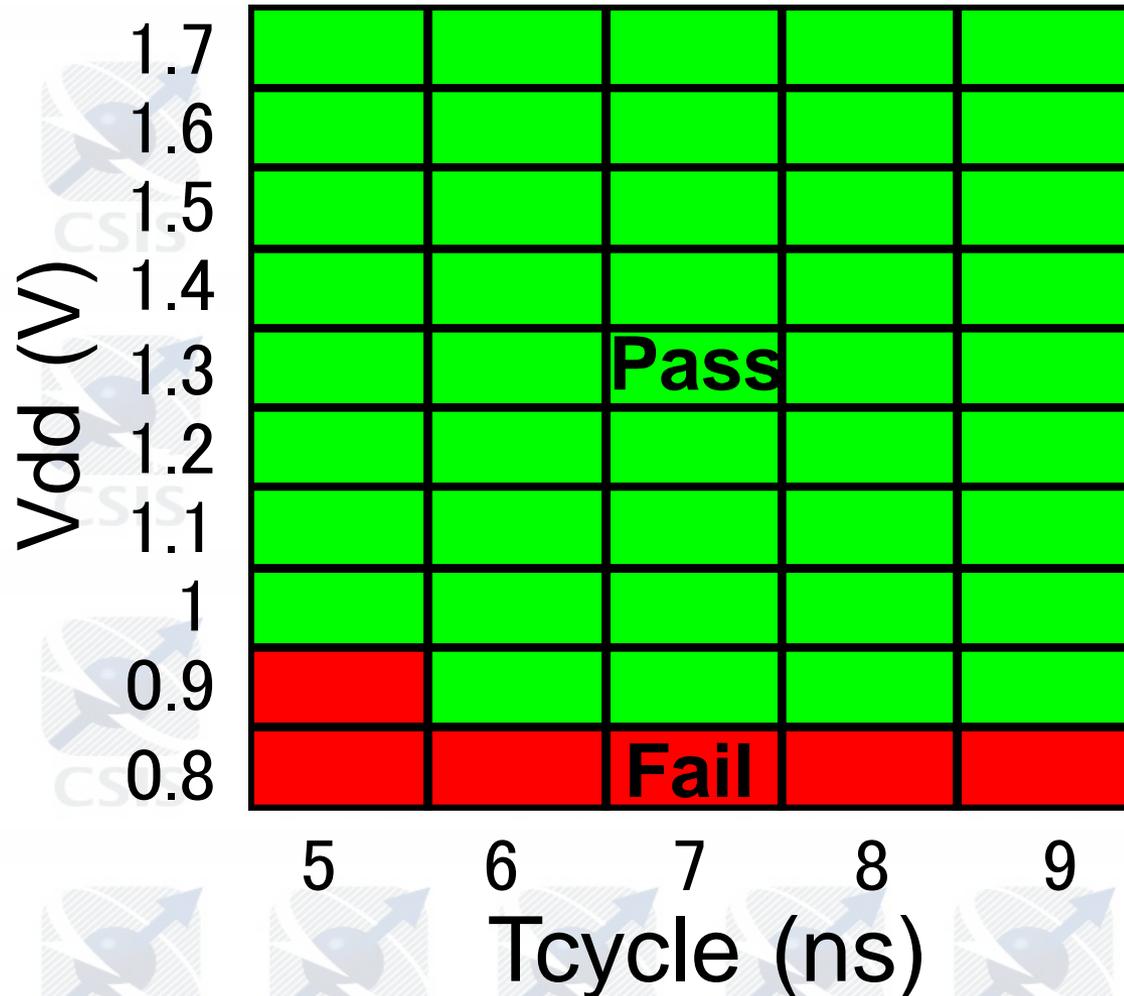


Technology	90 nm CMOS + DW Process
Cell size	6.6 $\mu\text{m}^2/\text{bit}$
Organization	128 word x 128 bit
Supply voltage	1.0 V
Search cycle time	5 ns

Measured 5-ns Search Waveform



Measured Search Cycle Time

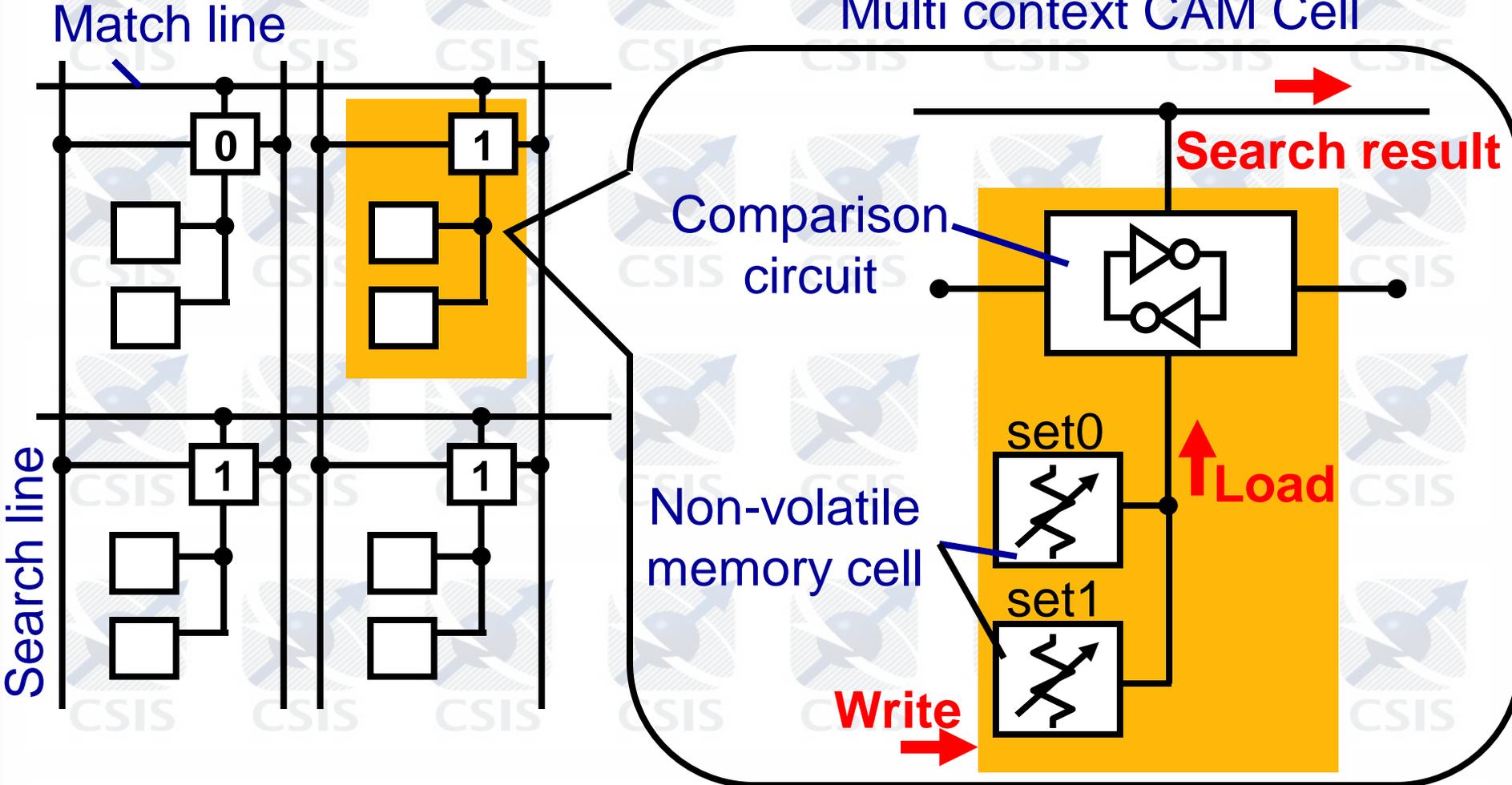


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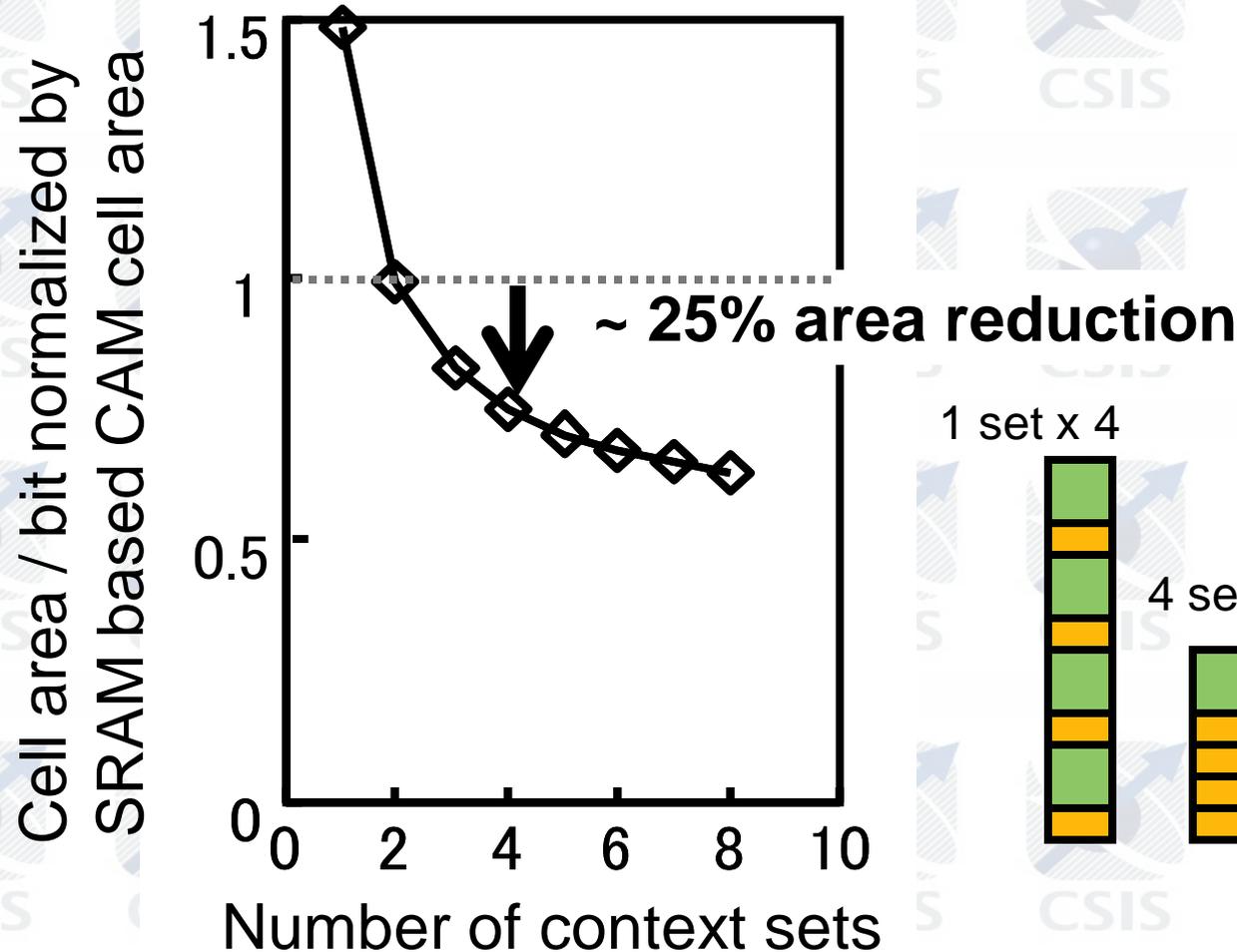
Basic Concept of Multi-context CAM

Multi context CAM Cell



- Non-volatile memory cells share comparison circuit → cell efficiency improves

Reduced Area of Multi-context CAM



1 set x 4



4 set x 1



Comparison circuit

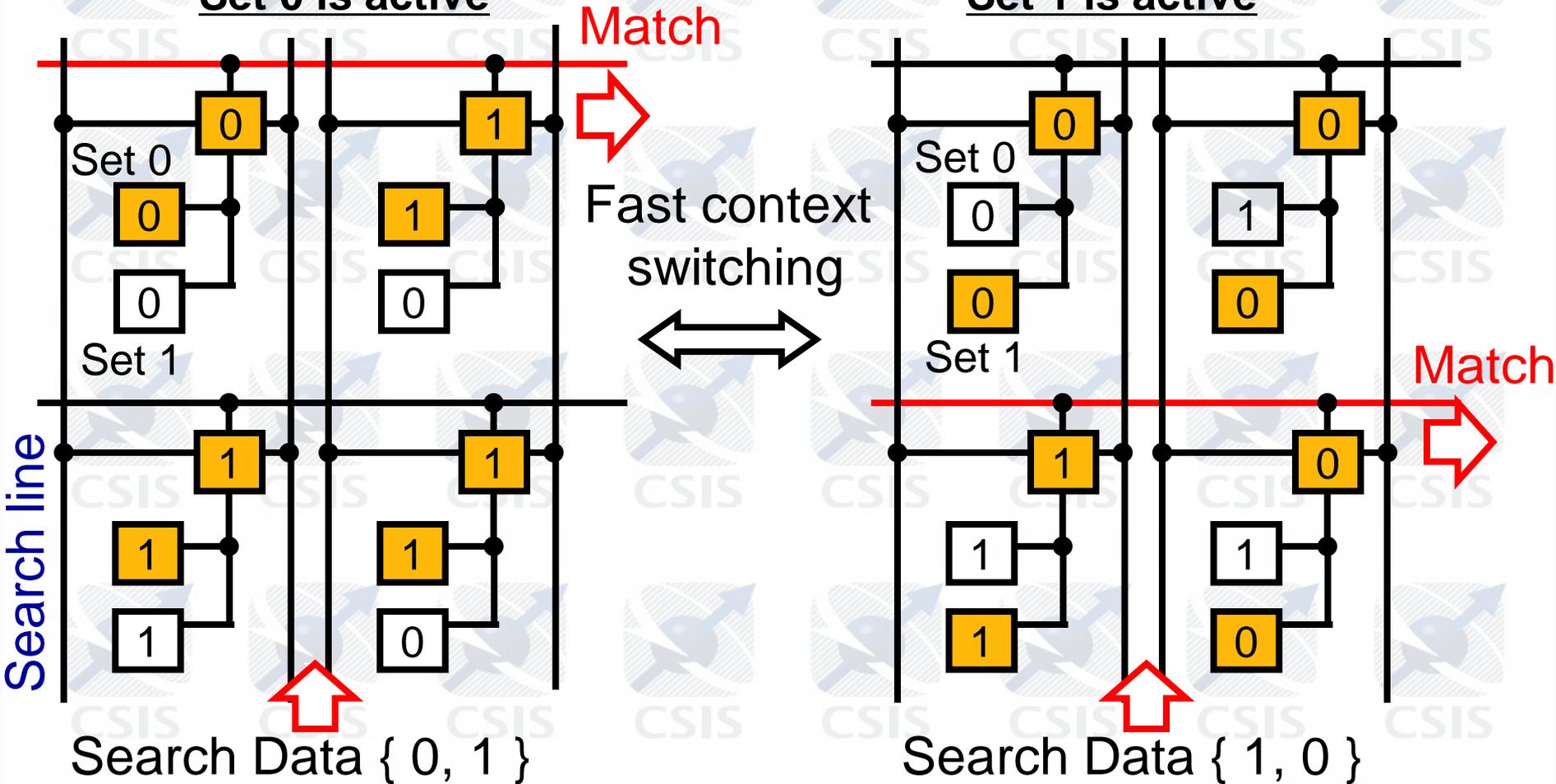
Non-volatile memory cell

- A 25% reduction in effective cell area was estimated with the CAM compared to an SRAM based CAM

Search Operation of Multi-context CAM

Set 0 is active

Set 1 is active



- Fast context switching
- Context switching cause increased overhead in power and delay

Application Example : Translation Look-aside Buffer

Process ID



Virtual Address



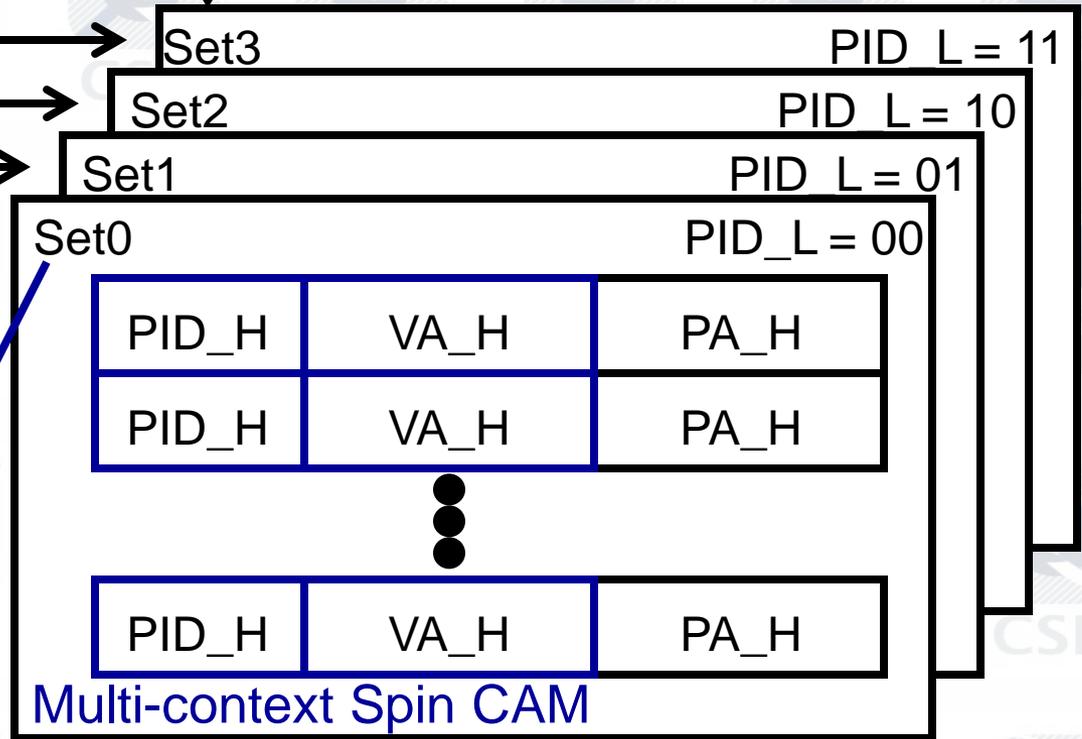
Time domain
pre-classification

- Low switching frequency
- Sets associated with PID



Small load overhead from MTJ

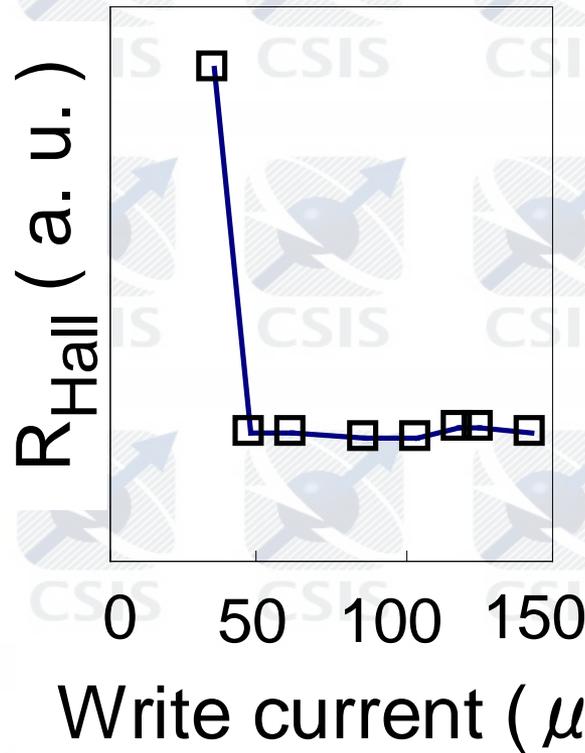
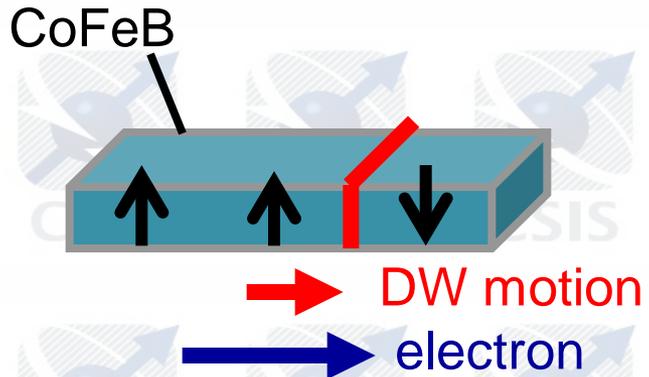
Avoid "cold start" with small area overhead



Physical Address



Domain Wall Motion in CoFeB



S. Fukami, Intermag 2011, GC-02.

- Domain wall moves with $\sim 50 \mu A$ current in CoFeB
- Future challenge is optimization and integration

Summary

- 16-Kb Spin CAM test chip
 - 5-ns search operation
- Multi-free layer domain wall (DW) cell
 - Fast read operation and small writing current
- 3-terminal device with shared write transistor
 - 6.6- μm^2 /bit cell area
- Multi-context Spin CAM
 - 25 % effective cell area reduction comparable to SRAM-based CAM
- Domain wall motion in CoFeB
 - Domain wall moves with $\sim 50 \mu\text{A}$ current