Embedded MRAM Technology For logic VLSI Application

November 7, 2011

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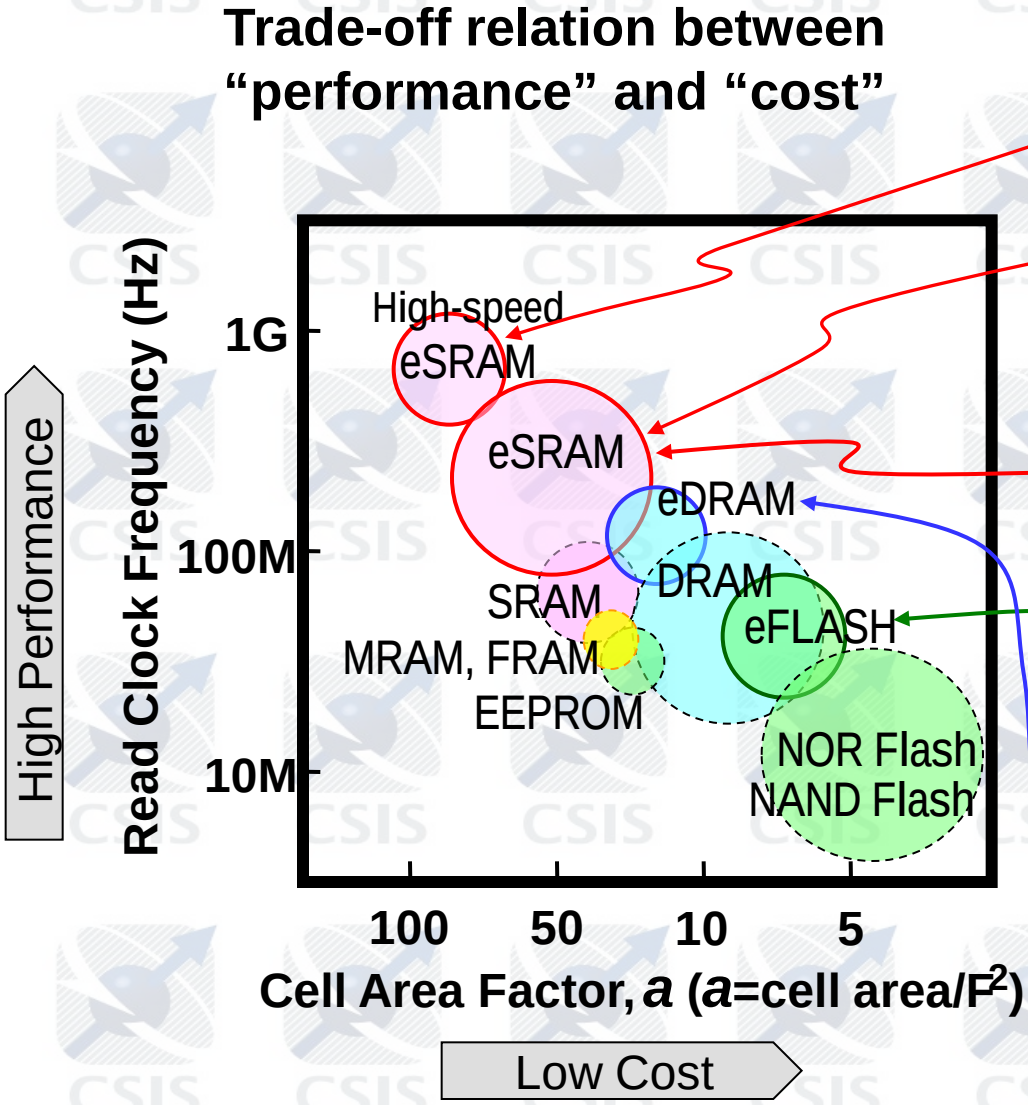
Work supported by the FIRST program of JSPS.

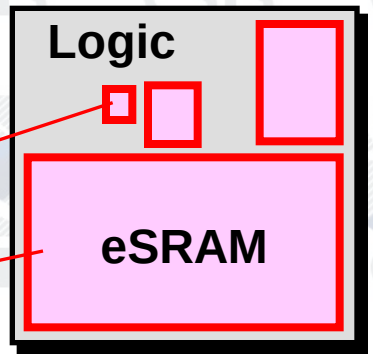
Existing Embedded Memory Market

WW Market @ 2010 World Semiconductor Trade Statistics	MOS Micro 61B (US$)		MOS Logic 77B (US$)
Applications	Micro-processor (PC, Server, …)	Micro-computer (4-32 bit MCUs)	ASIC, ASSP, FPGA (Mobile, Graphic, …)
Embedded Memory	SRAM L1-L3 cash	SRAM NOR-Flash	SRAM DRAM
Requirements	Ultra high speed RAM Large capacity RAM	High speed RAM Large capacity NVM	High speed RAM Large capacity RAM Wide band width RAM
Scaling Issues	Operation margin (Vth variation) Cell size scaling	Cell size scaling Reliable NVM	Cell size scaling Low operation power Low standby power
Key challenge	Low Power Voltage scaling	Wide temp. range Low cost	Voltage scaling Low cost

Memory Portfolio

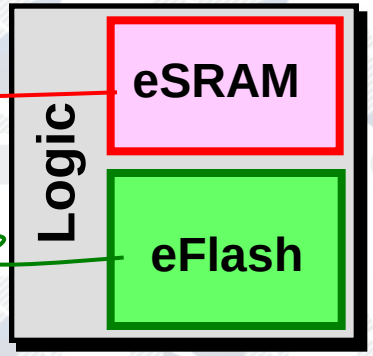
Trade-off relation between "performance" and "cost"





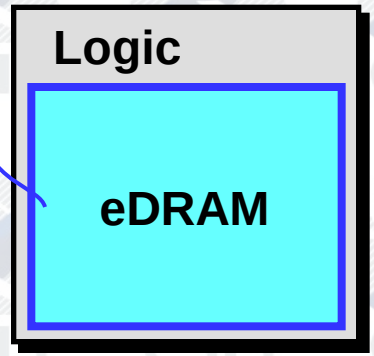
MPU, ASIC ...

- High Speed RAM
- Logic Compatibility
  - Low Voltage
  - Design



MCU

- High Speed NVM
- Various Application
  - Wide Temp. Range
  - High Reliability

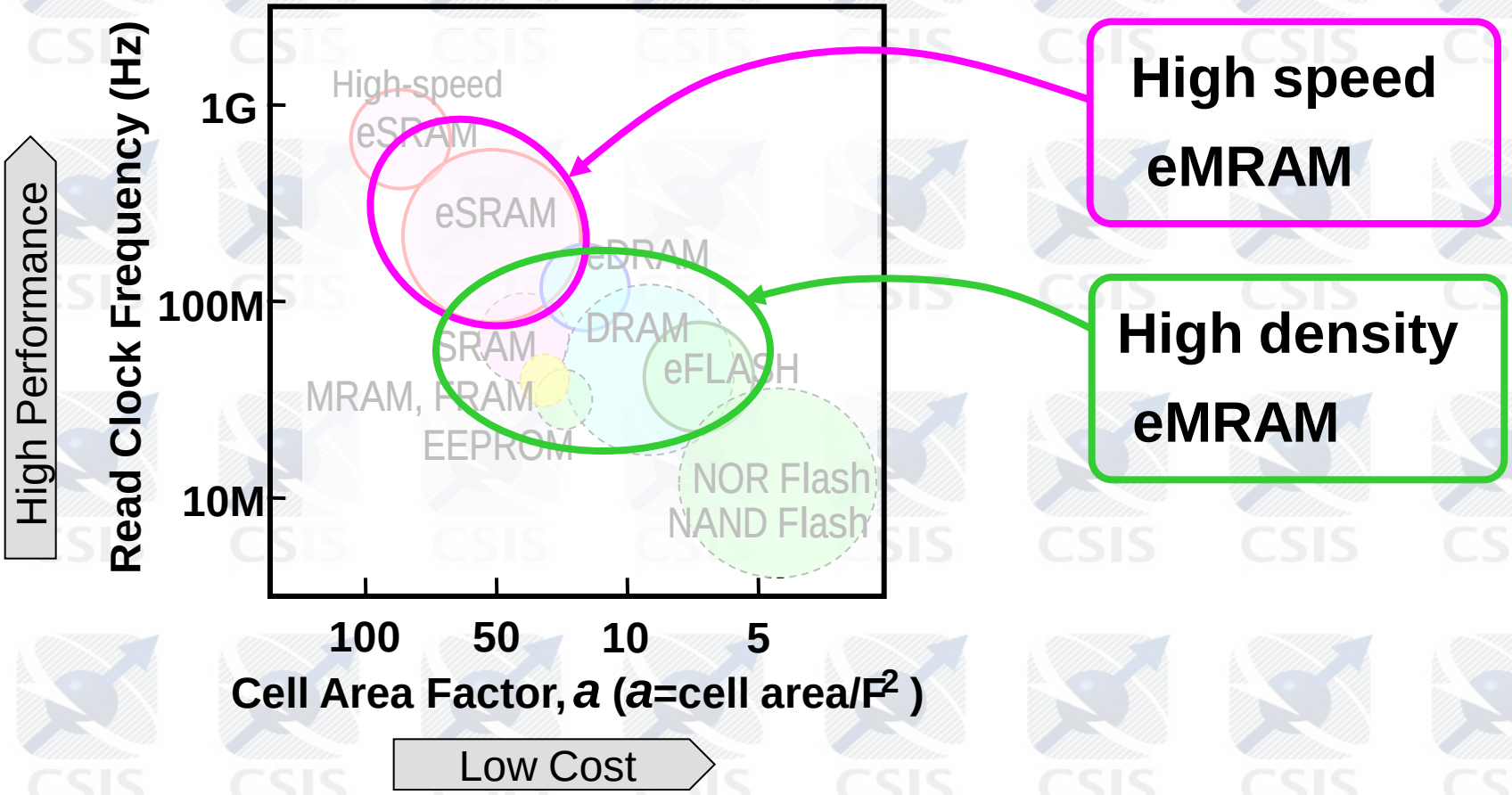


Graphics ...

- Wide Bandwidth
- Low Power
- Large Capacity

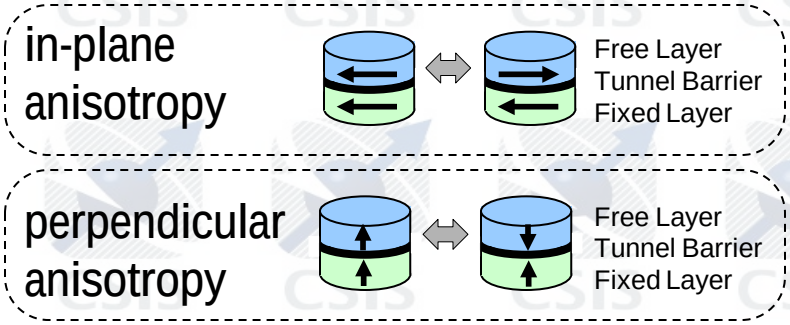
Alternative eMRAM

No universal embedded MRAM, but some types of MRAMs must be suitable for embedded applications.



Embedded MRAM Issues

- Standard CMOS Process compatible
- Suitable memory cell structure
  - Number of cell components; MTJ, transistor, wiring
  - Data write scheme; Magnetic Field, STT, ….
- MTJ: Magnetic Tunnel Junction
  - MR ratio
  - Magnetic anisotropy;

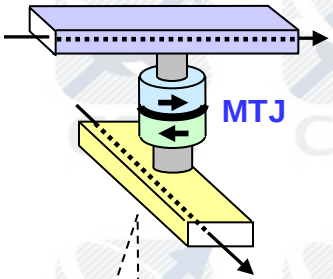
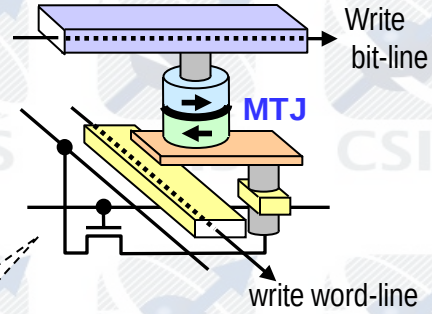
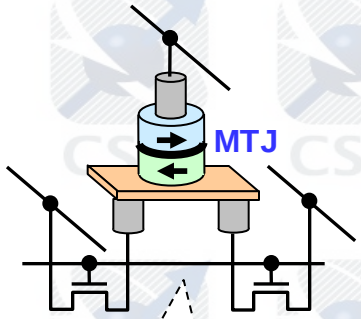
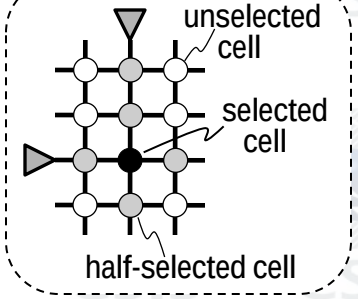
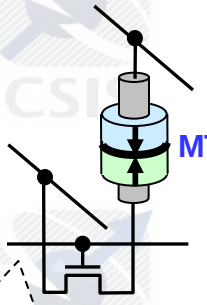
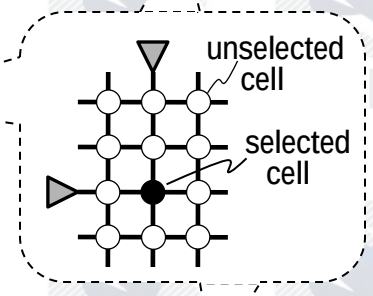
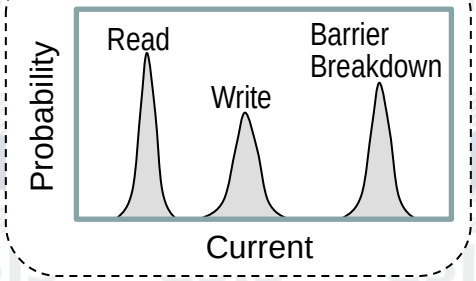
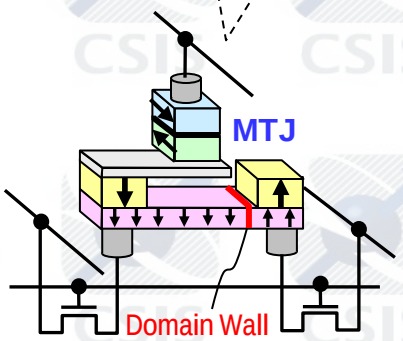


  - Materials of stacked thin magnetic layers and tunnel barrier film

CMOS Process Compatible

- **MTJs formed in back-end of line, BEOL**
  - CMOS characteristics unchanged
  - No Yoke (magnetic clad) lines
  - Cu & low-k interconnect applicable
  - 350 ºC thermal stability in BEOL fabrication process

Typical MRAM Cells

Data Write Scheme \ Cell Type	No Transistor 0Tr + 1MTJ	One Transistor 1Tr + 1MTJ	Two Transistors 2Tr + 1MTJ
Magnetic Field induced by write current through metal wires			
Spin Transfer Torque (STT) by current through MTJ			
Domain Wall Motion (DWM) by current through free layer			

High Density eMRAM Cell

Requirements

- Simple cell structure without snake path
- Random access read/write in cell array
- Scalable MTJ size & write current
- Large magneto-resistance(MR) ratio
- BEOL process temperature 350 ºC
- Reliability
  - Low tunnel current density
  - Non-volatality $\Delta = E/k_B T$

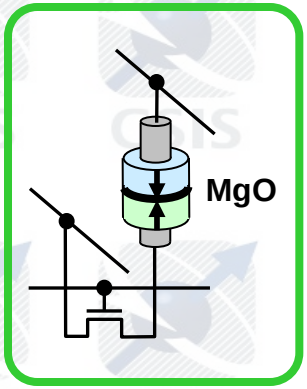
Choices

- 0Tr + 1MTJ
- **1Tr + 1MTJ**
- 2Tr + 1MTJ

- Magnetic Field
- **STT**
- **DWM**

- Al_2O_5
- **MgO**

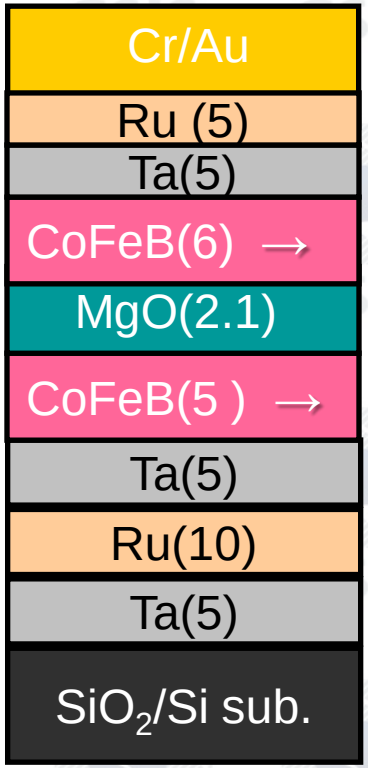
- In plane
- **Perpendicular**

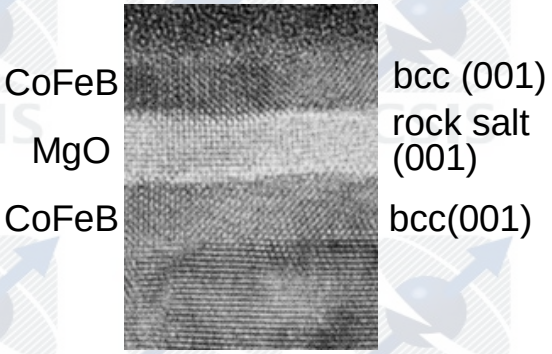


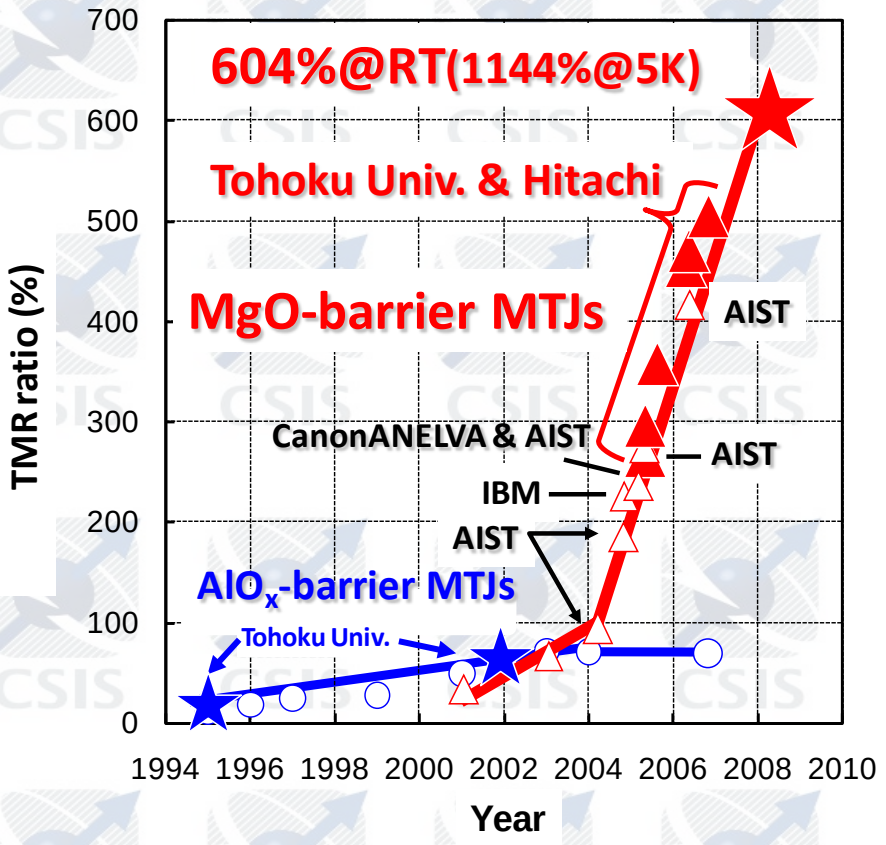
CoFeB/MgO/CoFeB MTJ

Large MR Ratio

In-plane anisotropy
pseudo-SV



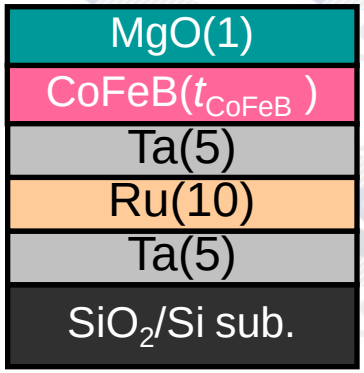




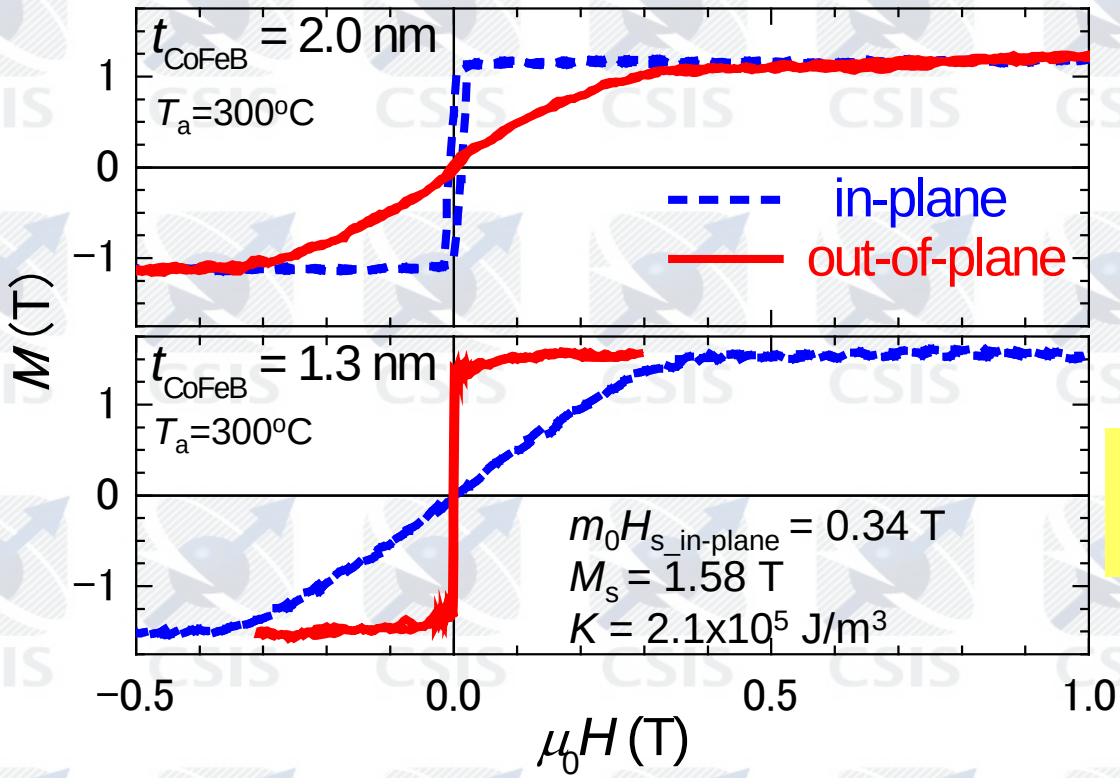
S. Ikeda et. al., Appl. Phys. Lett. **93**, 082508 (2008).

Dependence of t_{CoFeB} on Anisotropy

Perpendicular Anisotropy



T_a=300 °C,
4 kOe, 1h



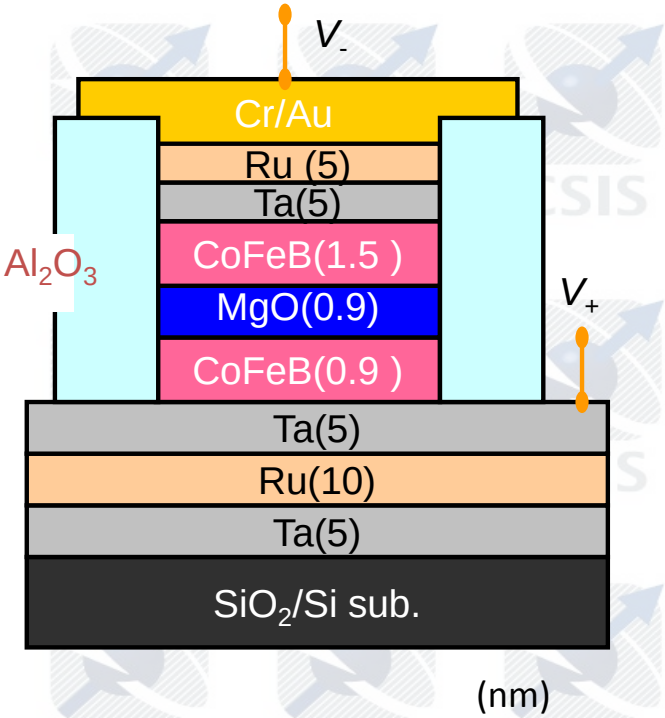
In-plane anisotropy

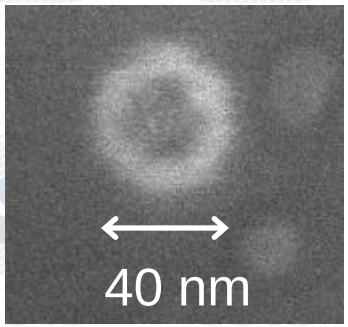
Perpendicular anisotropy

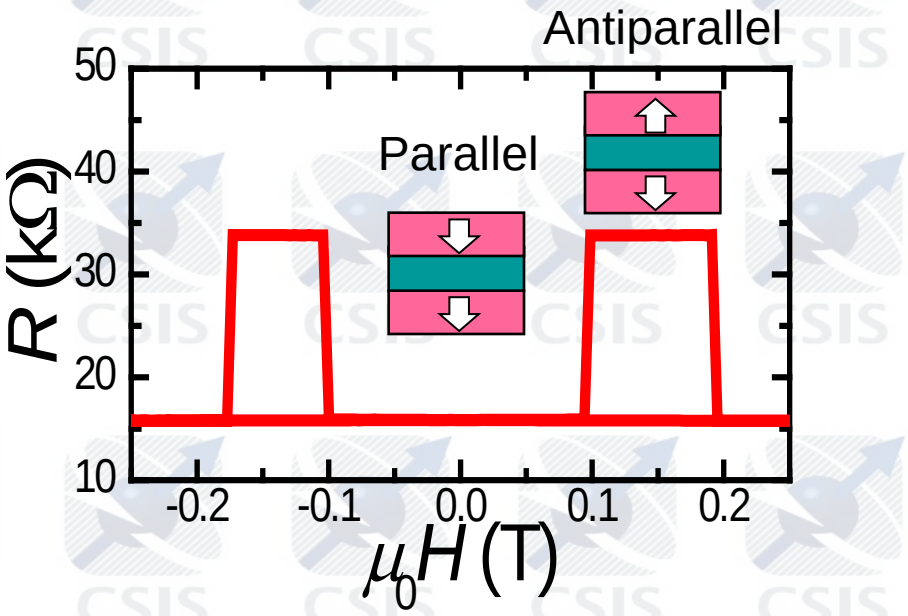
Ikeda et al., Nat. Mat., 9 (2010) pp.721-724

CoFeB/MgO/CoFeB MTJ

Perpendicular Anisotropy



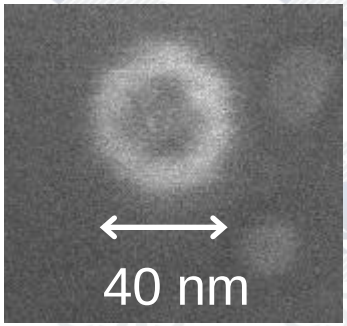


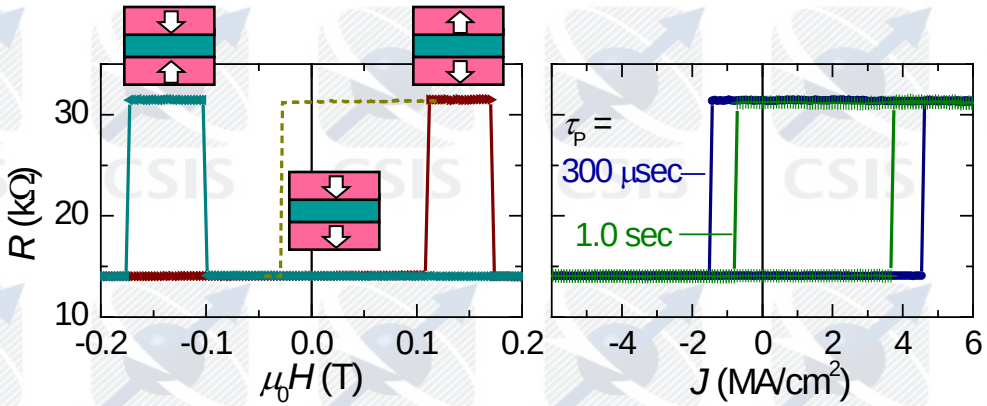


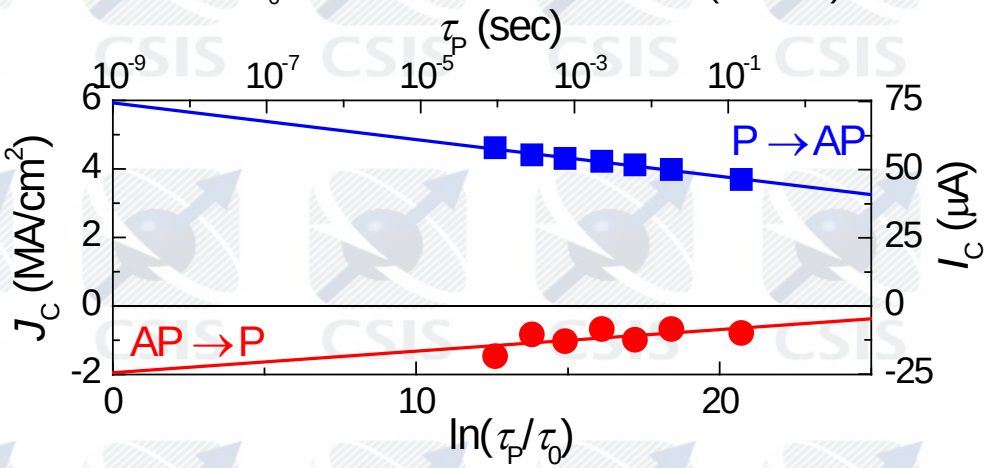
Ikeda et al., Nat. Mat., 9 (2010) pp.721-724

CoFeB/MgO/CoFeB MTJ

Spin Transfer Torque switching







Ikeda et al., Nat. Mat., 9 (2010) pp.721-724

TMR ratio =124%

RA = 18 Ωμm^2

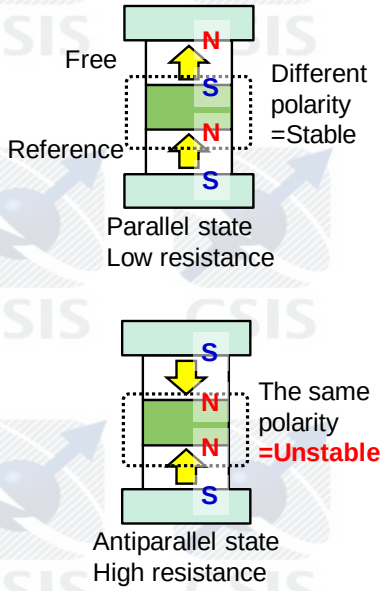
H_{shift} = 37 mT

I_{c0} = 50 μA (P-> AP)

- 20 μA (AP-> P)

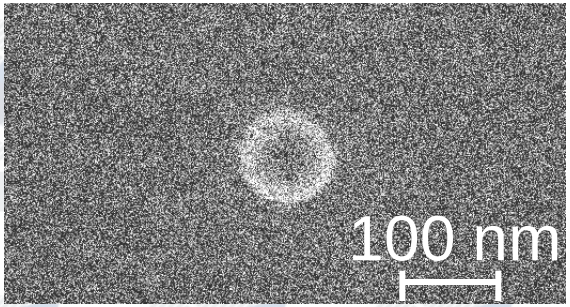
E/kBT = (Δ_P)

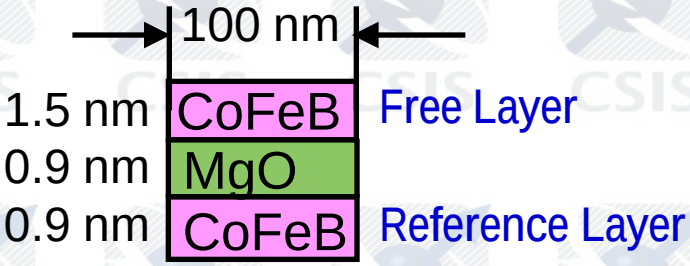
(Δ_{AP})

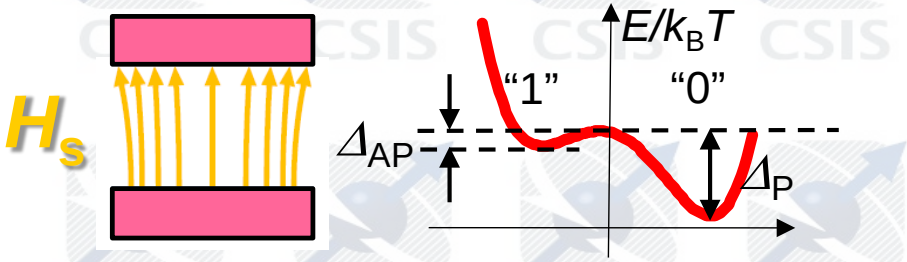


Stability Enhancement Structure

Conventional structure

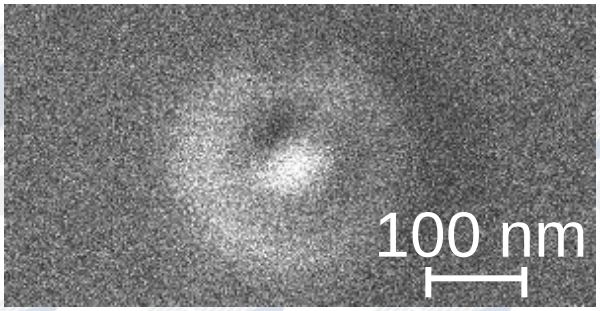


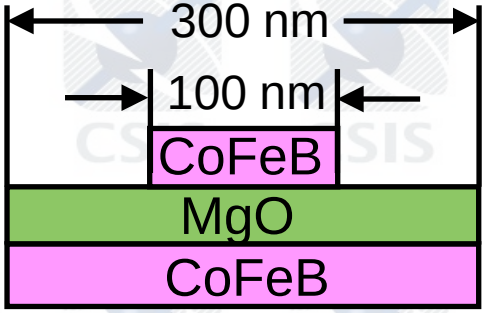


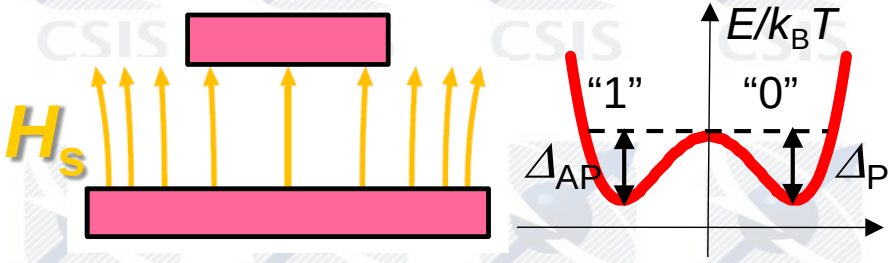


dipole interlayer coupling field

Stepped structure



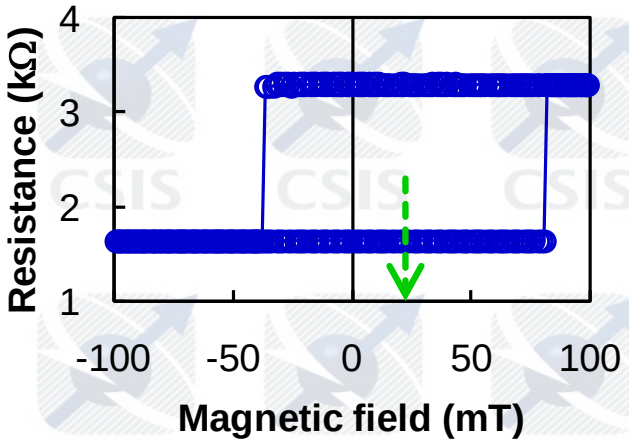




K. Miura et al., 2011 VLSI Technology, 11B-3.

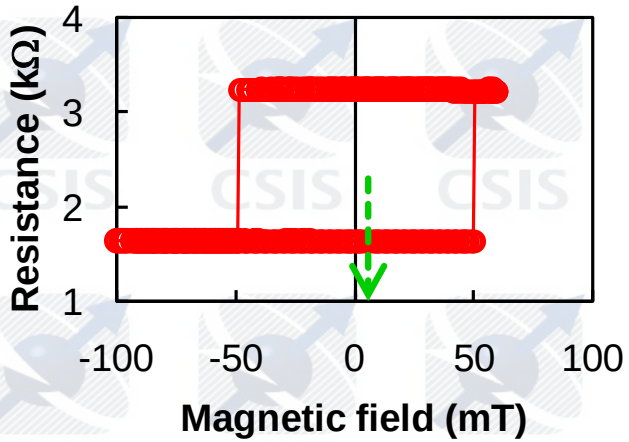
Stability Enhancement Structure

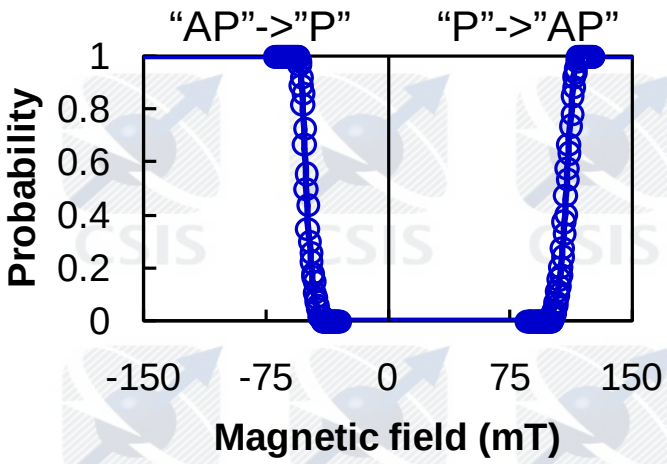
Conventional structure



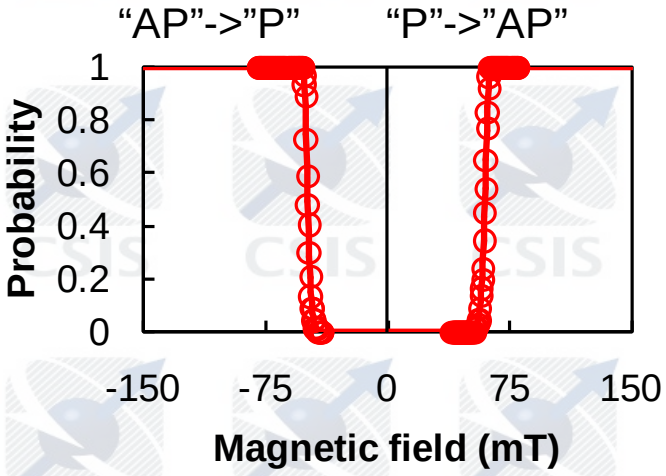
	Conventional	Stepped
TMR Ratio (%)	100	97
RA ($\Omega\mu m^2$)	13	13
H_s (mT)	22	5

Stepped structure





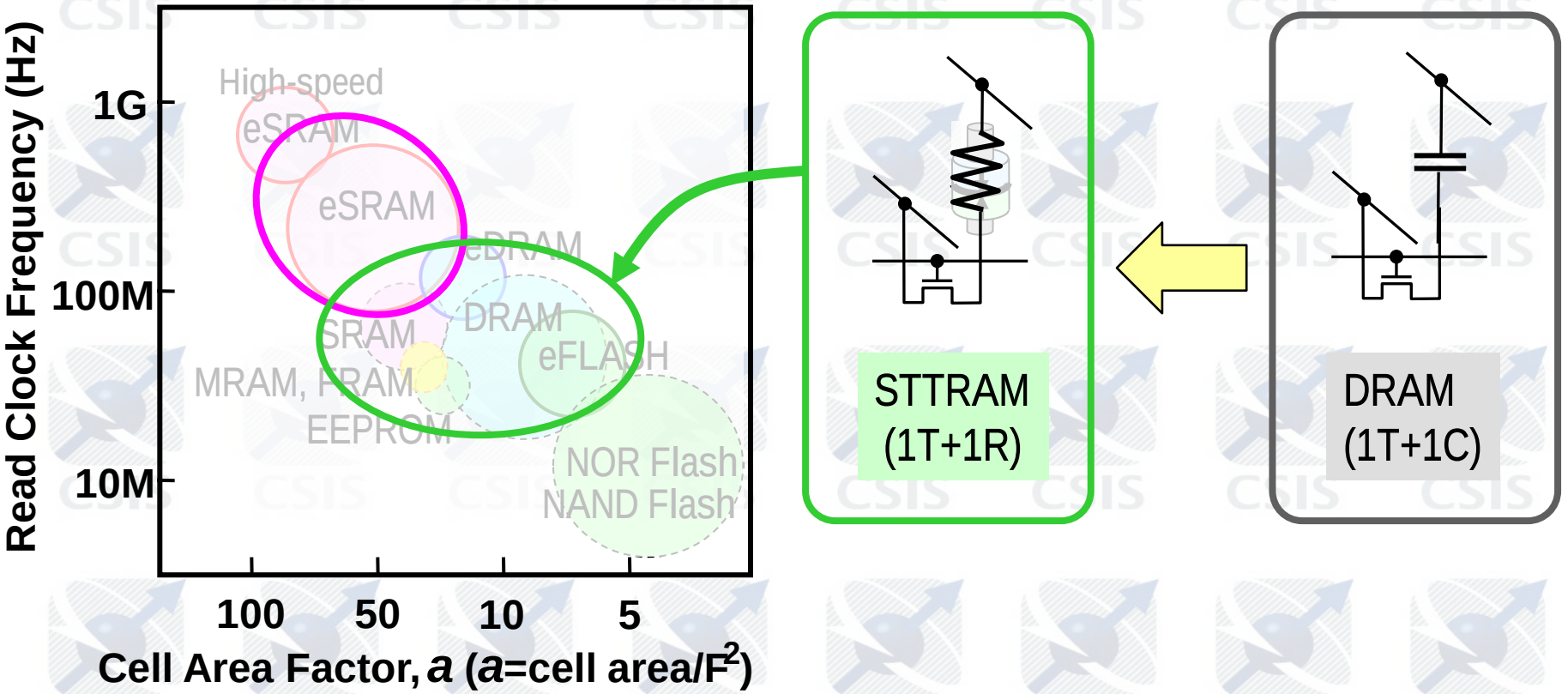
	Conventional	Stepped
Δ_P	71.2	72.9
Δ_{AP}	46.5	70.1



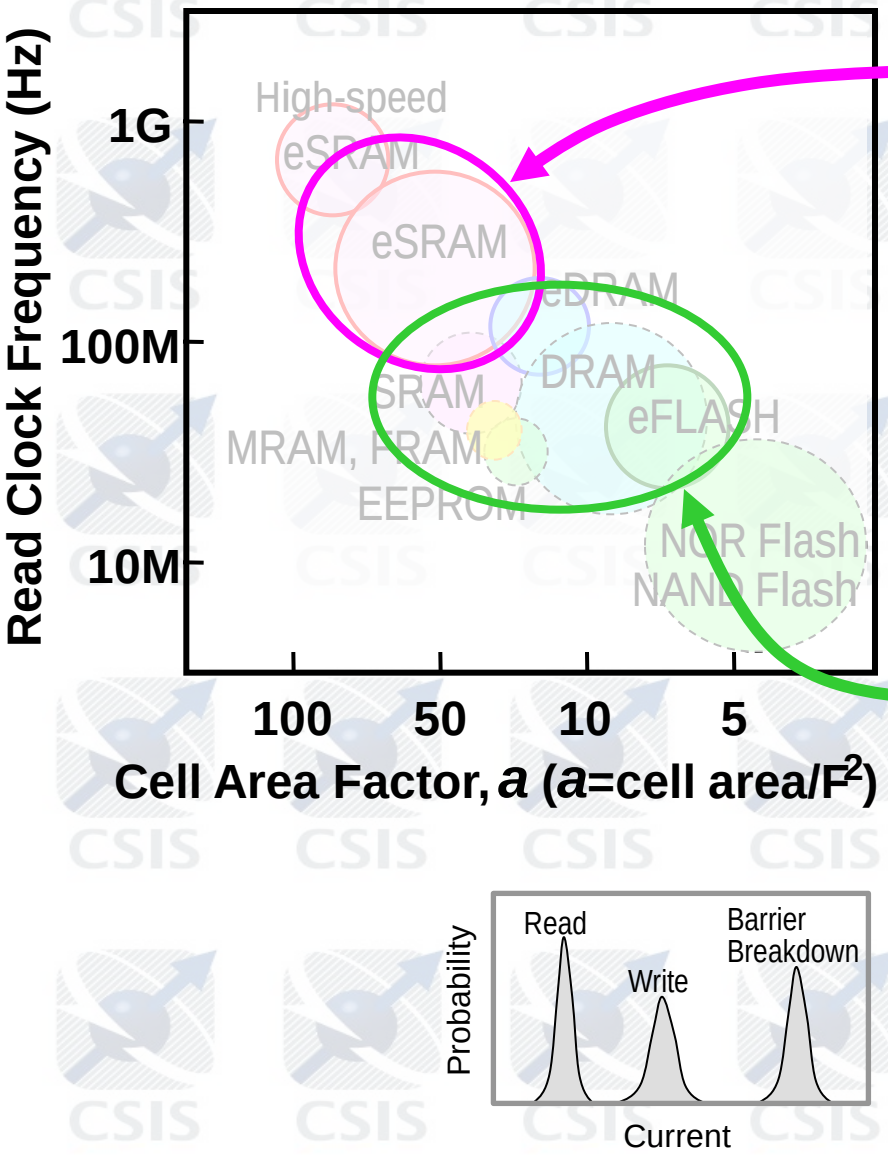
K. Miura et al., 2011 VLSI Technology, 11B-3.

Alternative High Density RAM

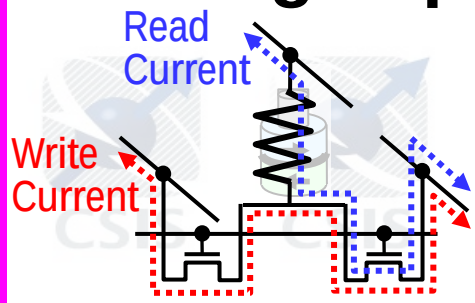
1T+1R STT MRAM must have potential to be substituted for not only embedded DRAM but also commodity DRAM.



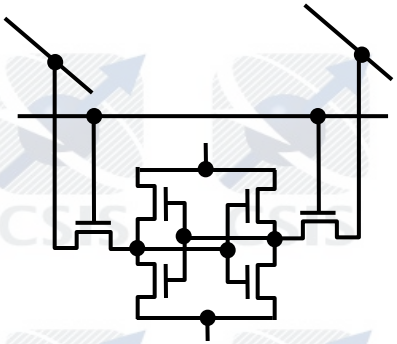
Alternative High Speed RAM



High speed RAM

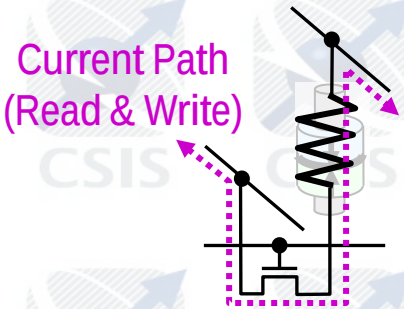


MRAM (2T+1R)

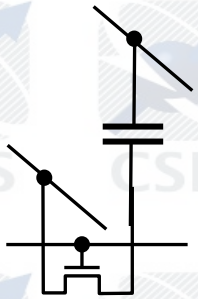


SRAM (6T)

High density RAM



STTRAM (1T+1R)



DRAM (1T+1C)

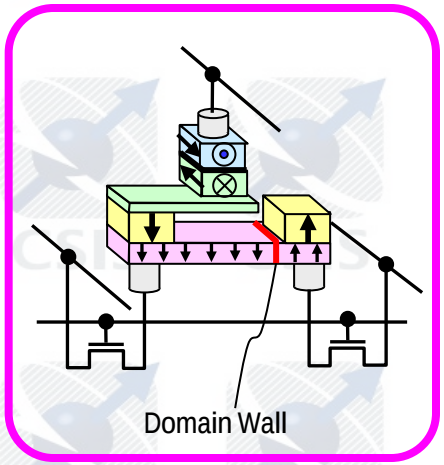
High Speed eMRAM Cell

Requirements

- Disturb free cell structure
- High speed random access read/write
- Scalable MTJ size & write current
- Large magneto-resistance(MR) ratio
- BEOL process temperature 350 ºC
- Reliability
  - Low tunnel current density
  - Non-volatality $\Delta = E/k_B T$

Choices

- 0Tr + 1MTJ
- 1Tr + 1MTJ
- 2Tr + 1MTJ ●
- Magnetic Field
- STT
- DWM ●
- Al_2O_5
- MgO ●
- In plane
- Perpendicular ●

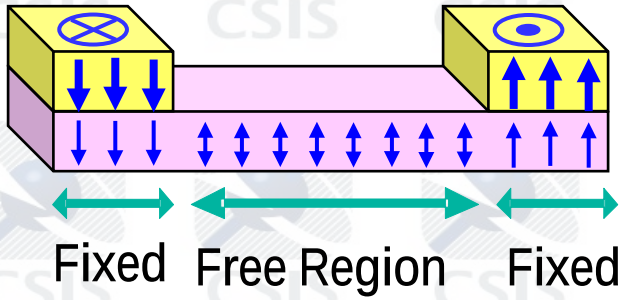


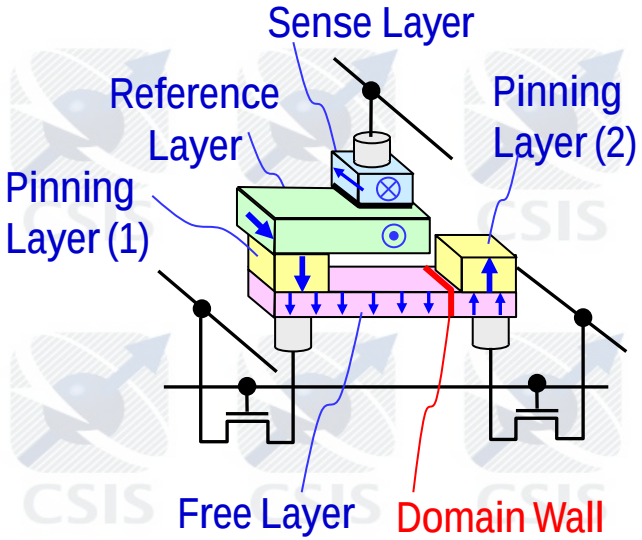
Domain Wall Motion(DWM) Writing

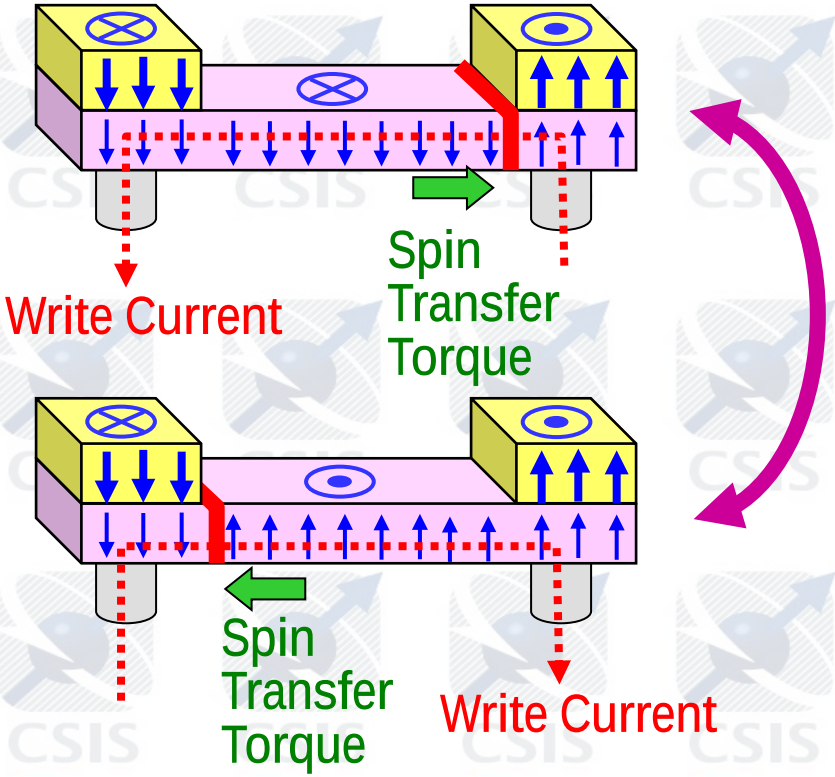
Perpendicular Anisotropy

- **Two Pinning Layers (PL)**
- **DWM Free Layer (FL)**

Hc(PL) >> Hc(FL)







R. Nebashi, et. al.,
Sym. VLSI Circuits. p. 300, 2011.

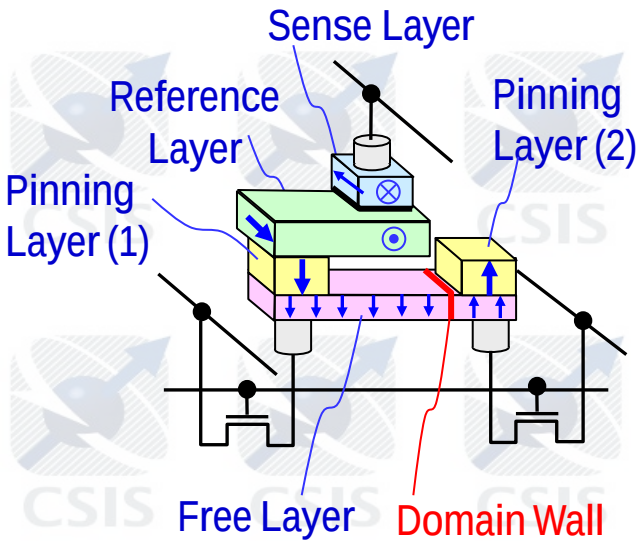
H. Honjo, et. al.,
56th MMM Conference, 2011.

Domain Wall Motion(DWM) Reading

In-plane Anisotropy

- **Sense Layer (SL)**
- **Reference Layer (RL)**

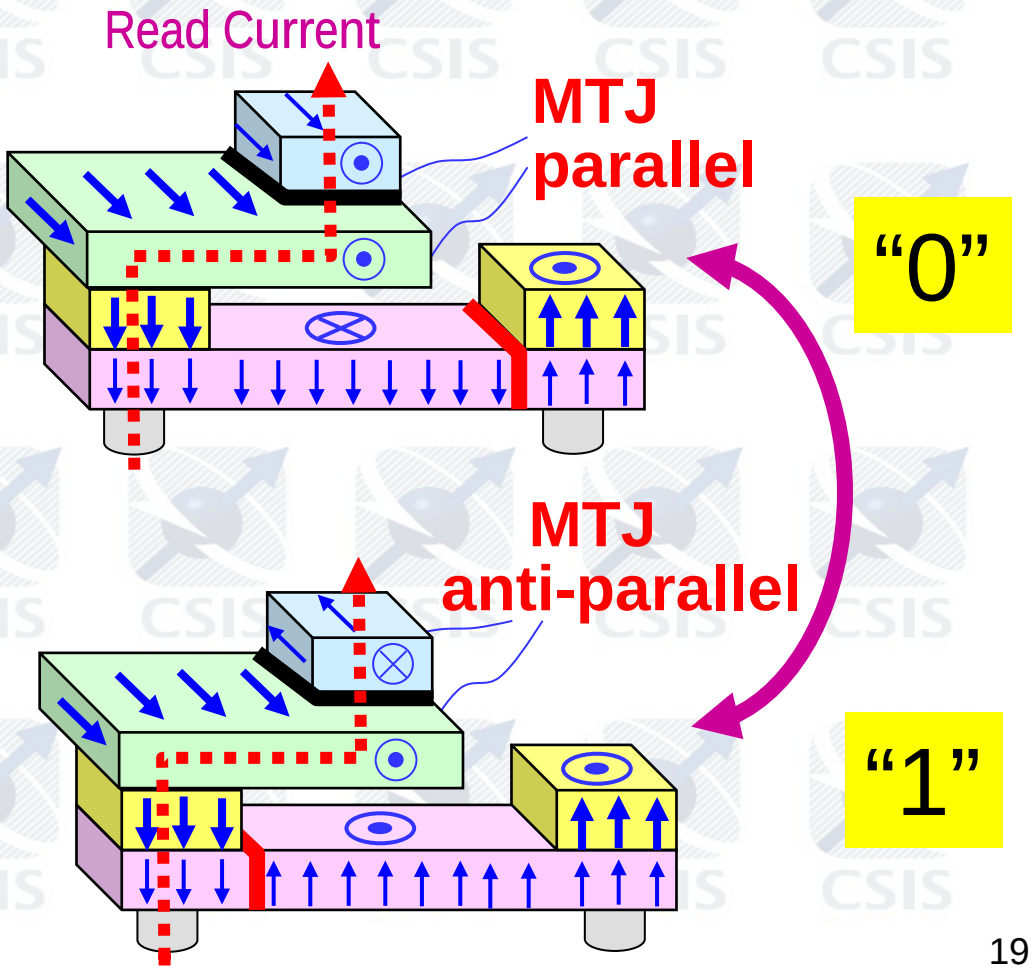
Hc(RL) >> Hc(SL)



R. Nebashi, et. al.,
Sym. VLSI Circuits. p. 300, 2011.

H. Honjo, et. al.,
56th MMM Conference, HR-10, 2011.

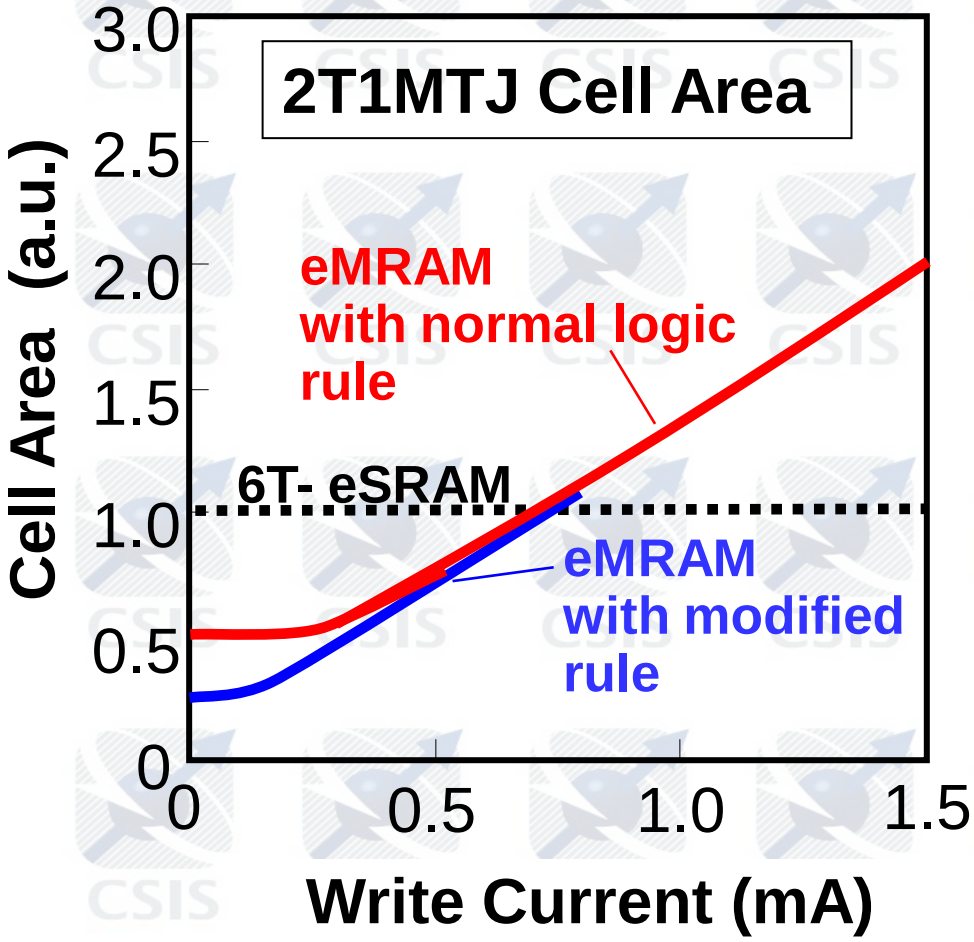
Sense layer magnetic direction is changed by stray field from DWM free layer

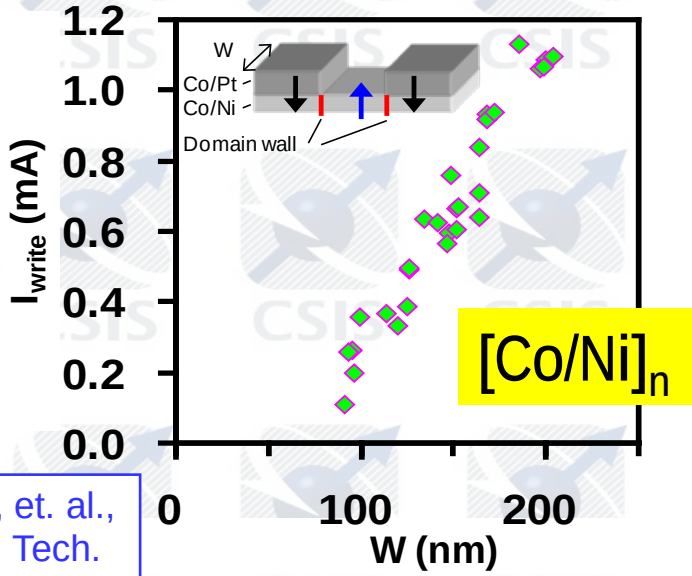


Write Current (Iw) Target

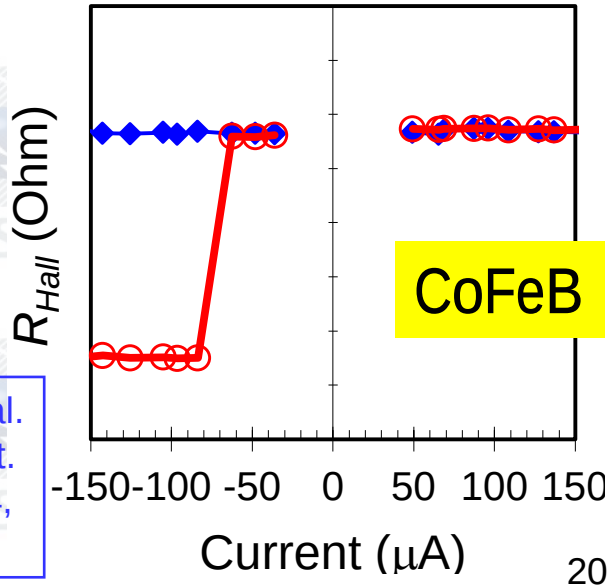
Iw < 0.5mA

Competitive in cost against eSRAM



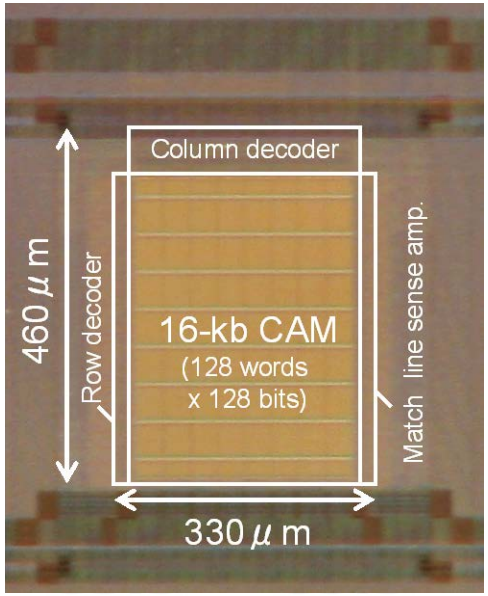


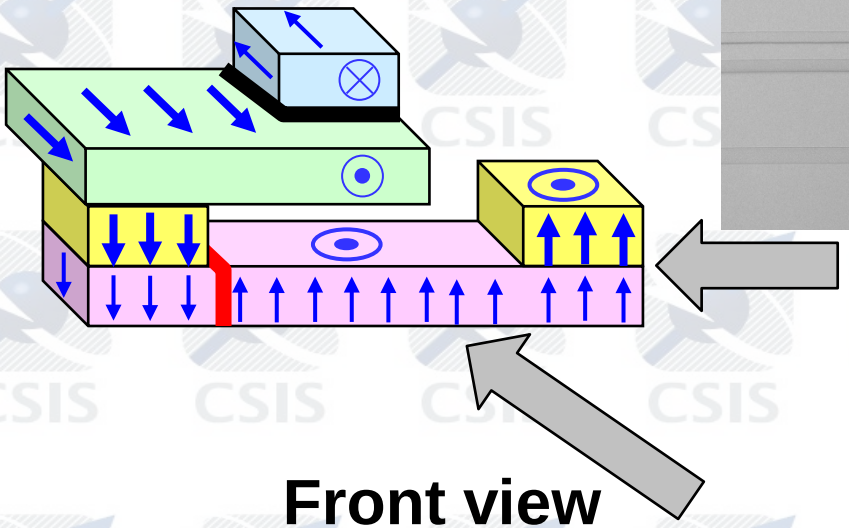
S. Fukami, et. al., Sym. VLSI Tech. p. 230, 2009.

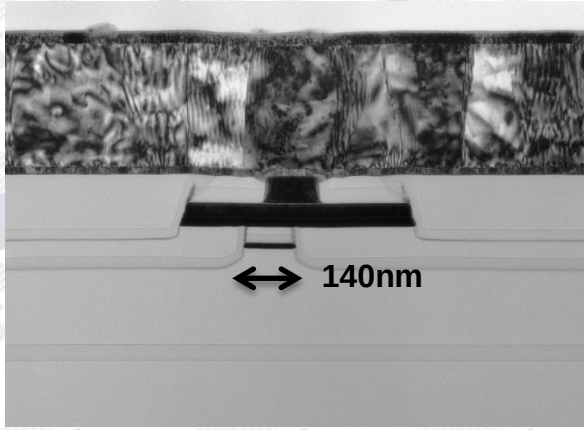


S. Fukami ,et. al. Appl. Phys. Lett. Vol. 98, 082504, 2011.

DWM NVM Fabrication



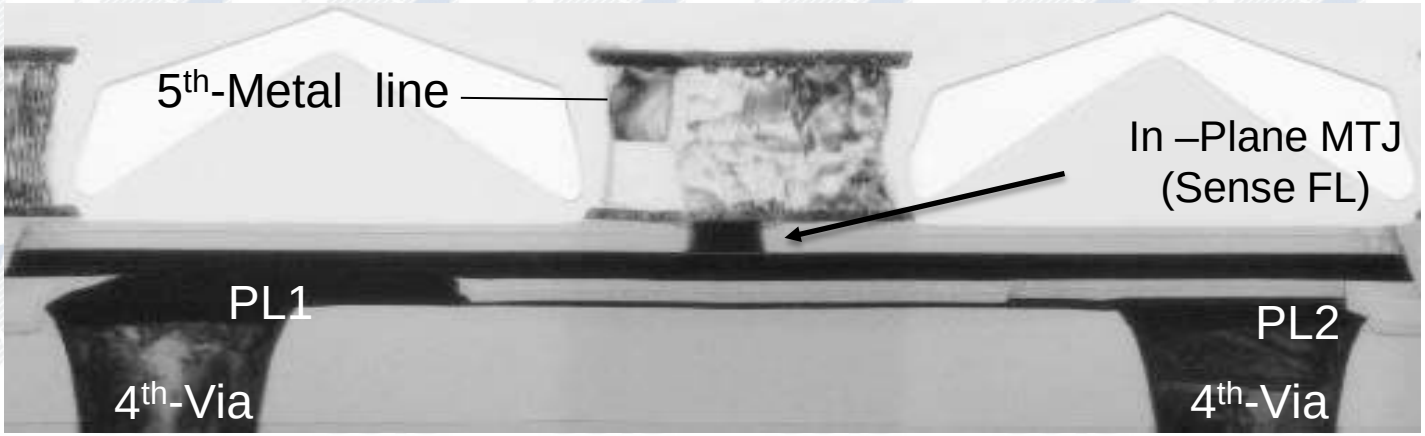




Side view

Front view

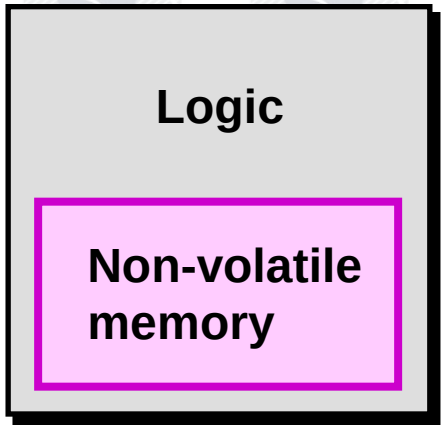
R. Nebashi, et. al., Sym. VLSI Circuits. p. 300, 2011.



FIRST Program Target

“Non-volatile logic-in-memory architecture”

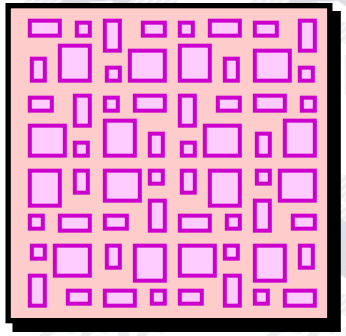
Logic with NVM



Static Power Reduction By NVM

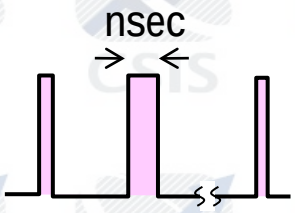
- 2 terminal STT
- 3 terminal MRAM
- ……

NV logic-in-memory



Storage / Logic merged

- NV full adder
- NV TCAM
- NV flip-flop
- NV ……
- NV ……



Dynamic Power Reduction

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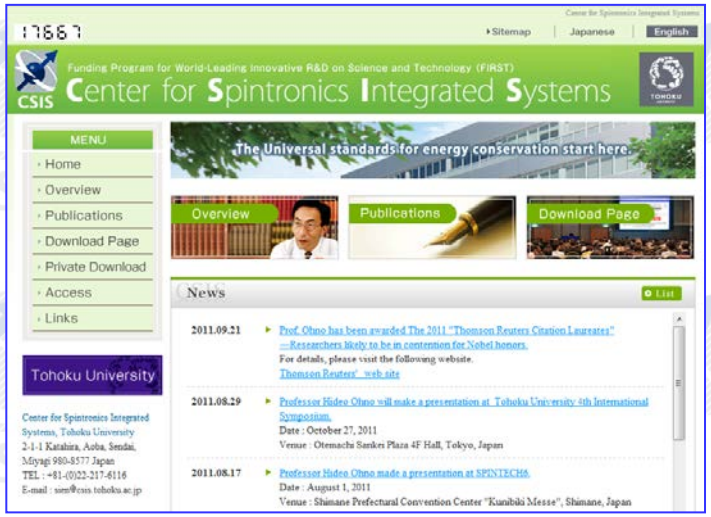
http://www.csis.tohoku.ac.jp/

New Energy Saving System on a Chip for Variety of applications



Summary

- **1T+1MTJ STT(Spin Torque Transfer) MRAM has the potentials for substitution of embedded DRAM to apply high density embedded NVM application.**
- **2T+1MTJ DWM(Domain Wall Motion) MRAM has the potentials for substitution of embedded SRAM to apply high speed NVM application.**
- **These embedded MRAM technology leads to "logic-in-memory architecture" for future new energy saving SoC(System on a Chip).**

Acknowledgements

This research is granted by the Japan Society for the Promotion of Science (JSPS) through the “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program),” initiated by the Council for Science and Technology Policy (CSTP). Prof. Hideo Ohno has been conducting the program “Research and Development of Ultra-low Power Spintronics-based VLSIs“ as the core researcher.

Thanks to

K. Miura, H. Yamamoto, K. Misunuma, H. D. Gan, M, Endo, S. Kanai, J. Hayakawa, F. Matsukura, M. Yamanouchi, J. Hayakawa, R. Kiizumi, S. Fukami, T. Suzuki, K. Nagahara, N. Ohshima, Y. Ozaki, S. Saito, R. Nebashi, N. Sakimura, H. Honjo, K. Mori, C. Igarashi, S. Miura, N. Ishiwata, K. Kinoshita, Y. Nakatani, Y. Tsuji, R. Nebashi, N. Sakimura, H. Honjo, K. Mori, H. Tanigawa, S. Miura, and T. Sugibayashi