Fully Parallel 6T-2MTJ Nonvolatile TCAM with Single-Transistor-Based Self Match-Line Discharge Control

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Outline

- Background & Purpose
- 6T-2MTJ-Based NV-TCAM Cell and Test Chip Fabrication
- Design Example of Low-Power NV-TCAM Using Three-Level Segmented Match-Line Scheme
- Conclusions

Background

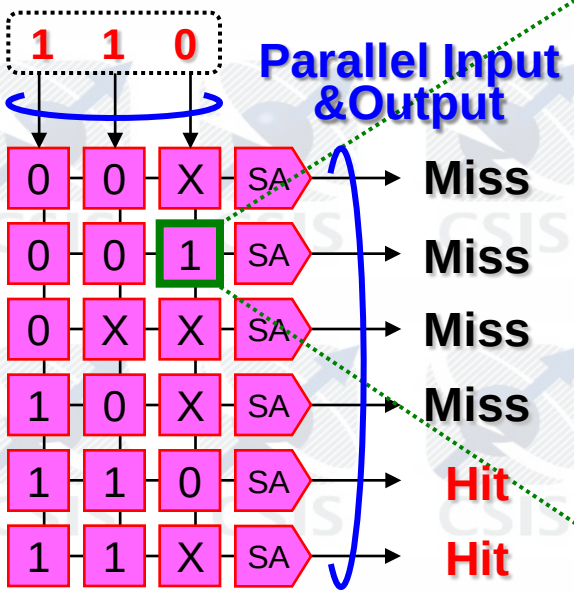
TCAM (Ternary Content-Addressable Memory)

Fully Parallel equality-search ⇨ **High-speed pattern matching**

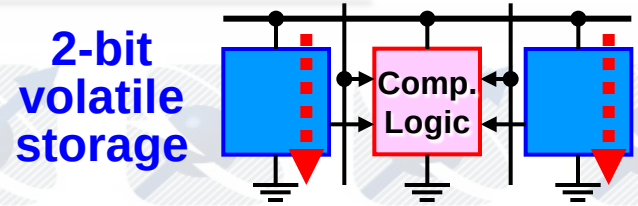
Applications: *Database, virus checker, network router, etc.*

Demands: ***Large capacity***, ***Low-power consumption***

Search word



TCAM cell structure



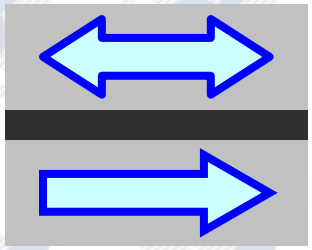
Problems:

- Many device counts of TCAM cell
  ⇨ **Large cell area**
- Increasing leakage current
  ⇨ **High standby power**

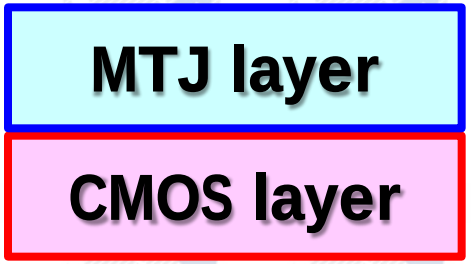
Purpose : Realize a compact and low-power TCAM

Merits of MTJ-Based Nonvolatile Logic-in-Memory

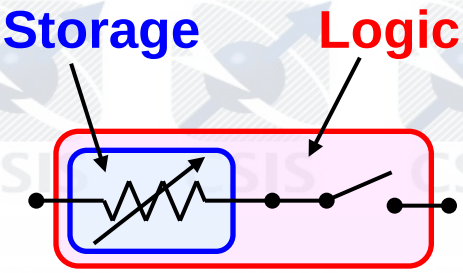
MTJ device



Hardware structure



Function



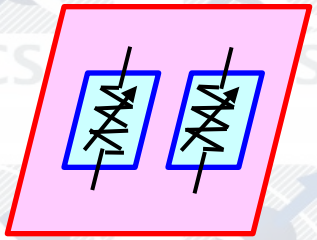
- **Nonvolatile storage**
  → Perfectly cut off the power supply.
  → **Low standby power**
- **3D-stacking structure**
  → Greatly reduce area overhead of storage.
  → **Compact**
- **CMOS/MTJ-hybrid logic**
  → Merge storage and logic functions.
  → **More compact**

Nonvolatile Logic-in-Memory structure is suitable for a compact and low-standby-power TCAM.

Approaches for a Compact and Low-Power TCAM

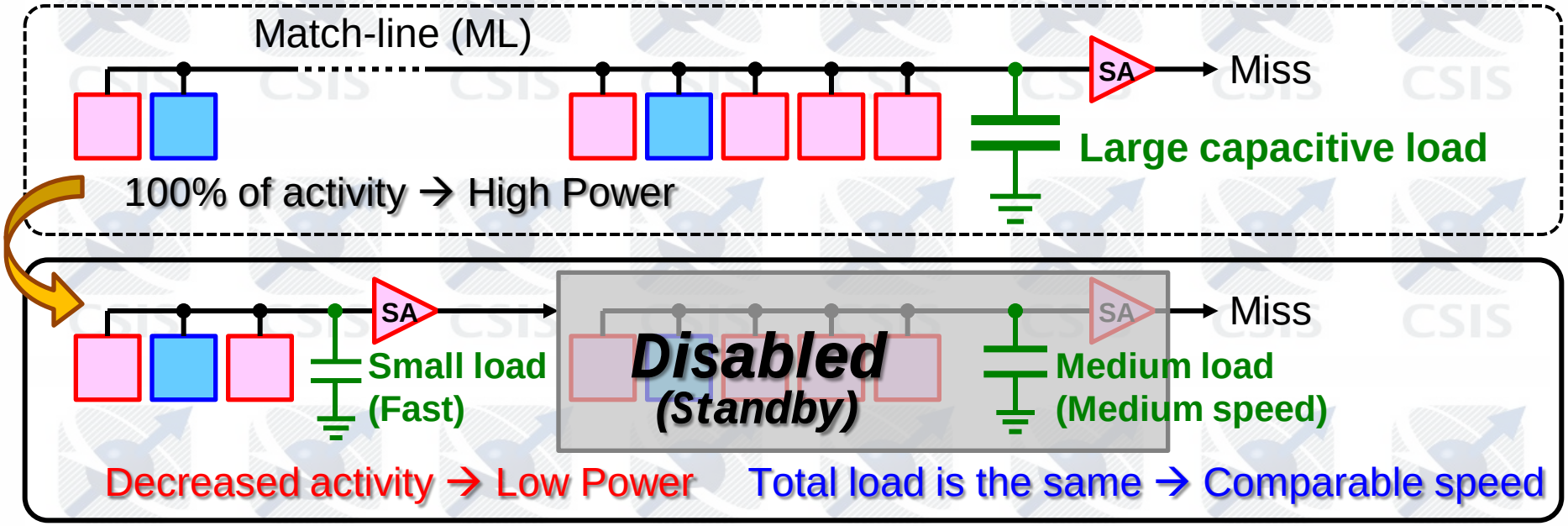
- **For Large Capacity (Small Cell Size)**
  - Utilize nonvolatile logic-in-memory
    - 3D-stacking structure
    - CMOS/MTJ-hybrid logic

→ Compact (& Nonvolatile)



NV-TCAM cell

- **For Low Power (with maintaining search speed)**
  - Eliminate wasted cell activation → Low active power
  - Power OFF at standby state using nonvolatility → Low standby power



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- **6T-2MTJ-Based NV-TCAM Cell and Test Chip Fabrication**
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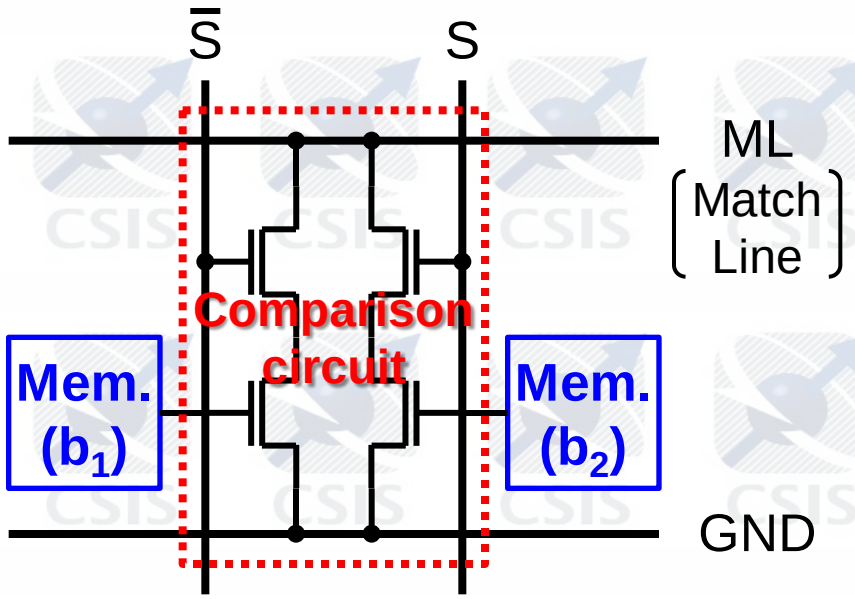
Conventional TCAM Cell

Cell circuit



2-bit Volatile Mem. (SRAM cells)

⇨ Large cell size (16Tr. or 12Tr.)

⇨ High leakage

Truth table

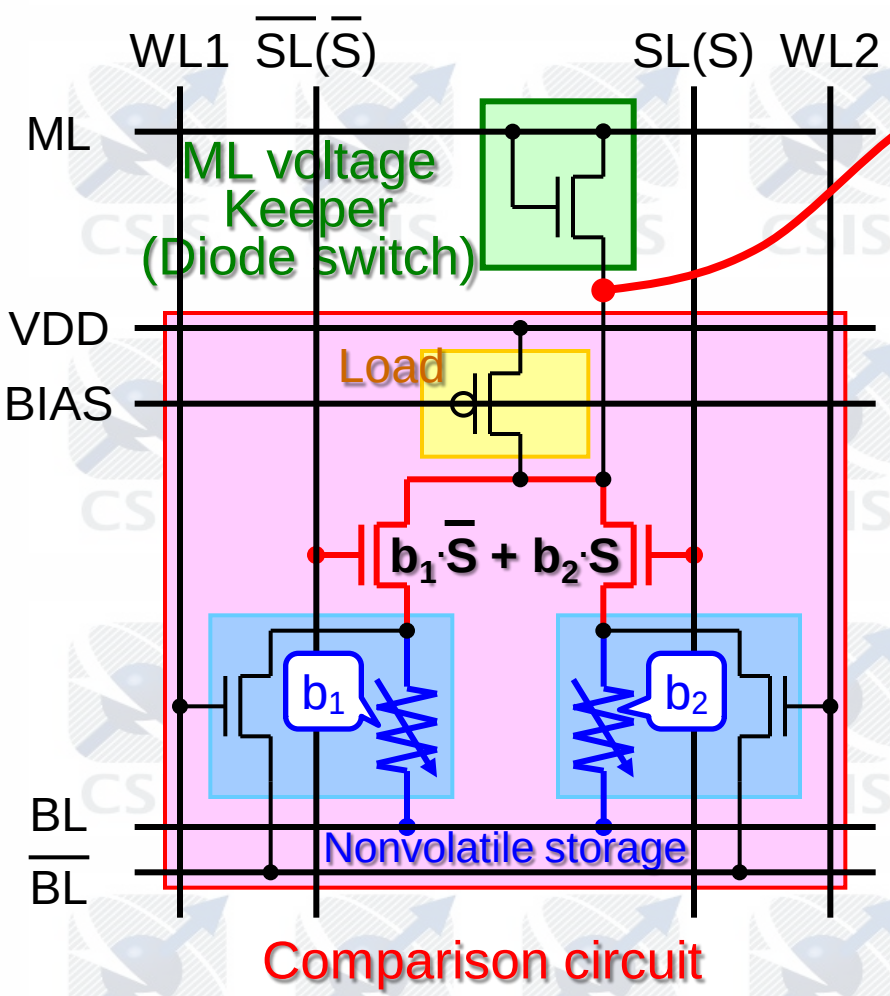
Stored data		Input	Matched result
B	(b_1, b_2)	**S**	**ML**
0	(0, 1)	**0**	**1** (Hit)
		1	**0** (Miss)
1	(1, 0)	**0**	**0** (Miss)
		1	**1** (Hit)
X (**Don't care**)	(0, 0)	**0**	**1** (Hit)
		1	Masked

$$ML = b_1 \cdot \overline{S} + b_2 \cdot S$$

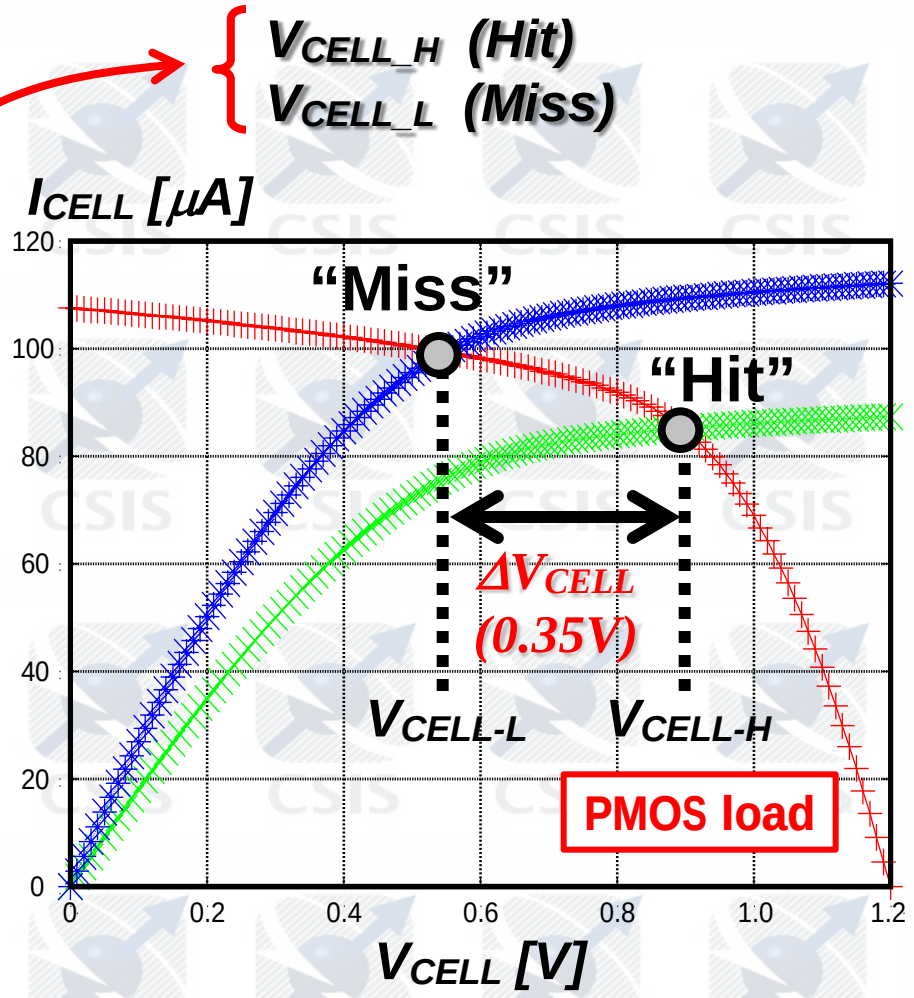
It is desirable to realize a **compact** and **nonvolatile** TCAM cell.

Proposed NV-TCAM Cell

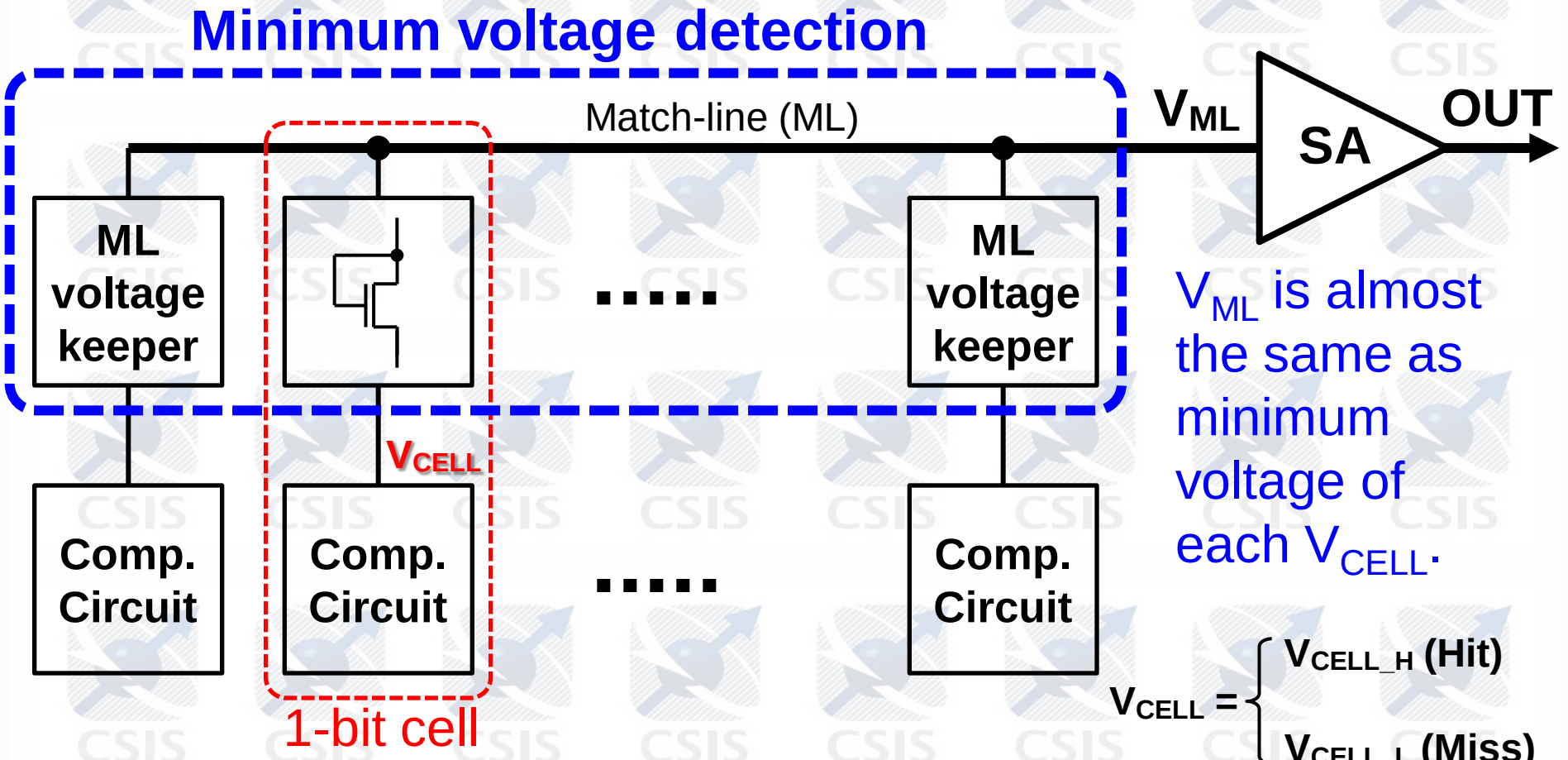
6T-2MTJ NV-TCAM cell



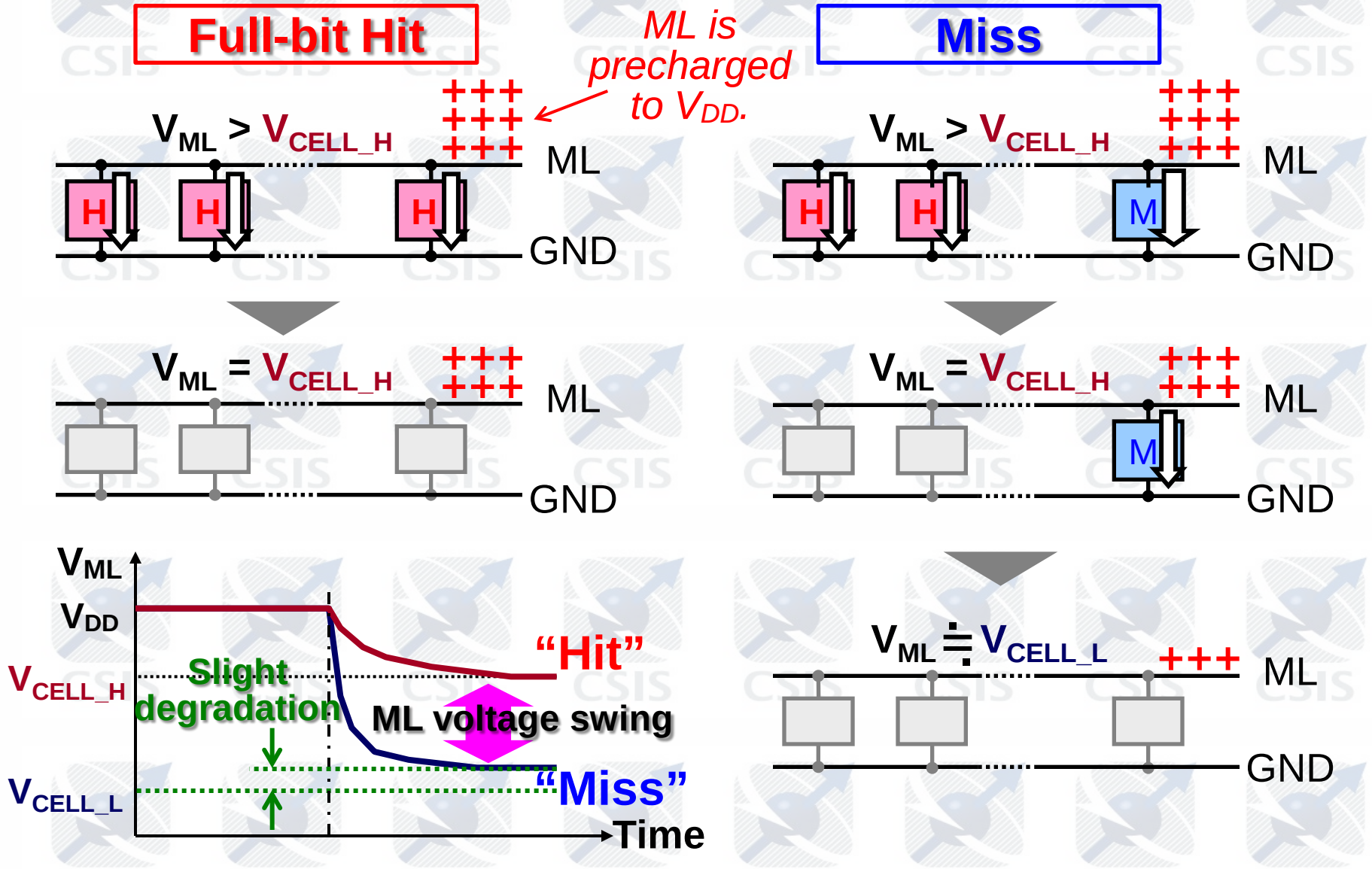
Measured I-V char.



Mechanism of ML voltage keeper

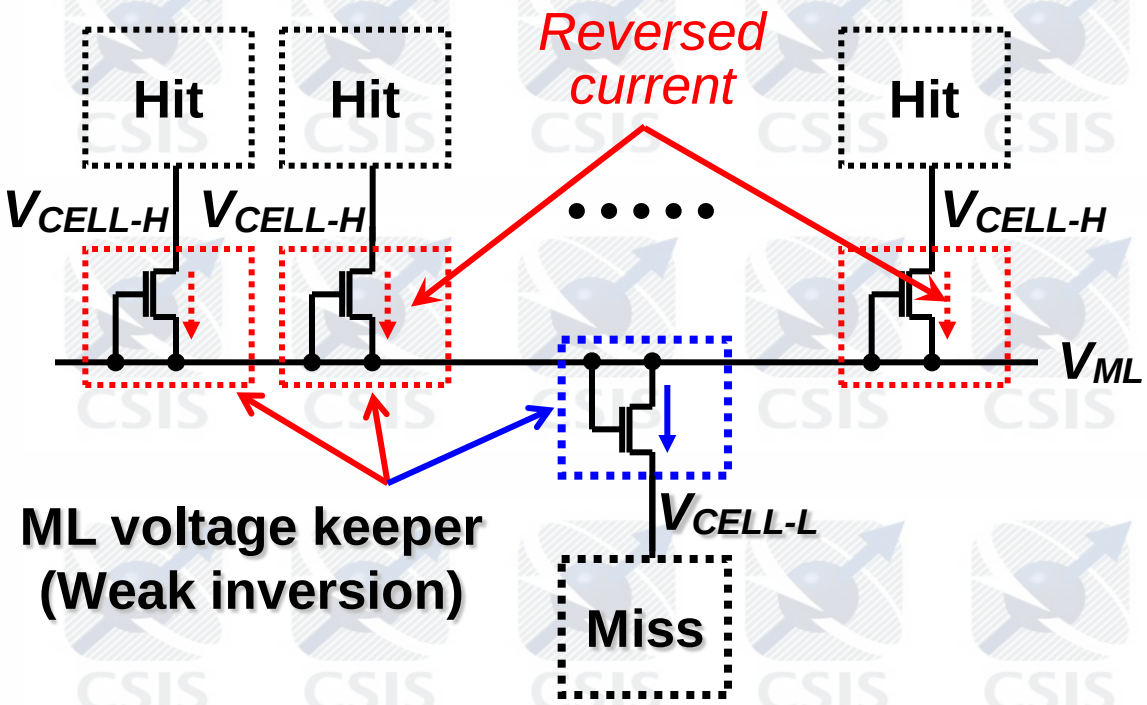


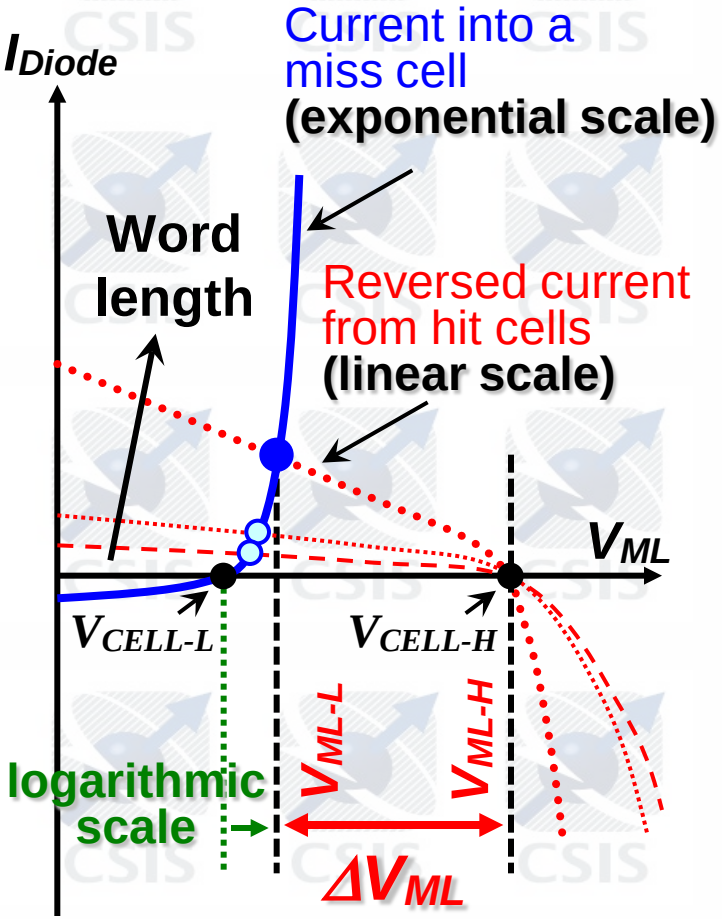
Self Match-Line Discharge Control in Word Circuit



Match-Line Voltage Swing

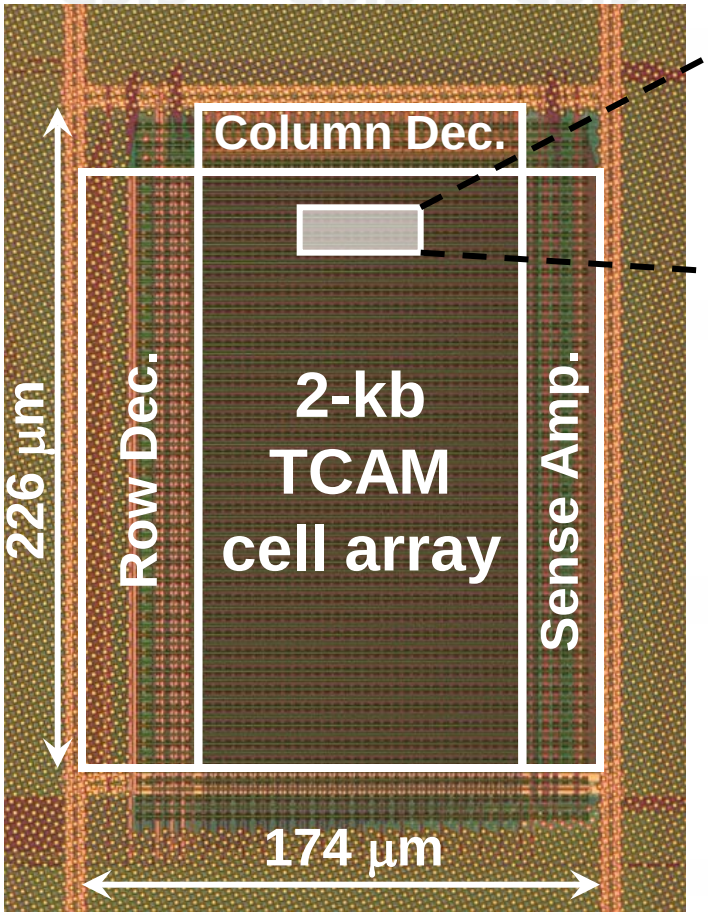
1-bit miss detection (worst case)

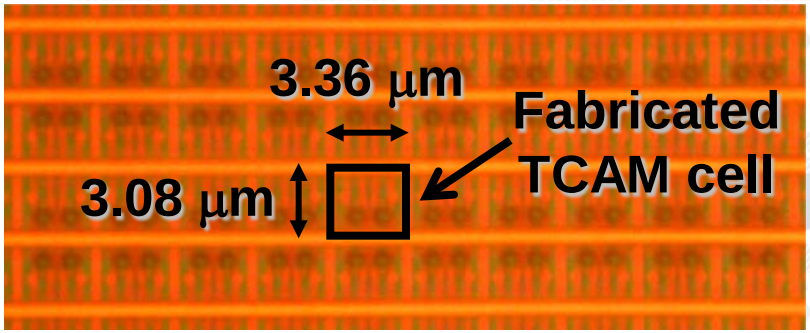




Sufficient ML voltage swing can be obtained even in longer word circuit.

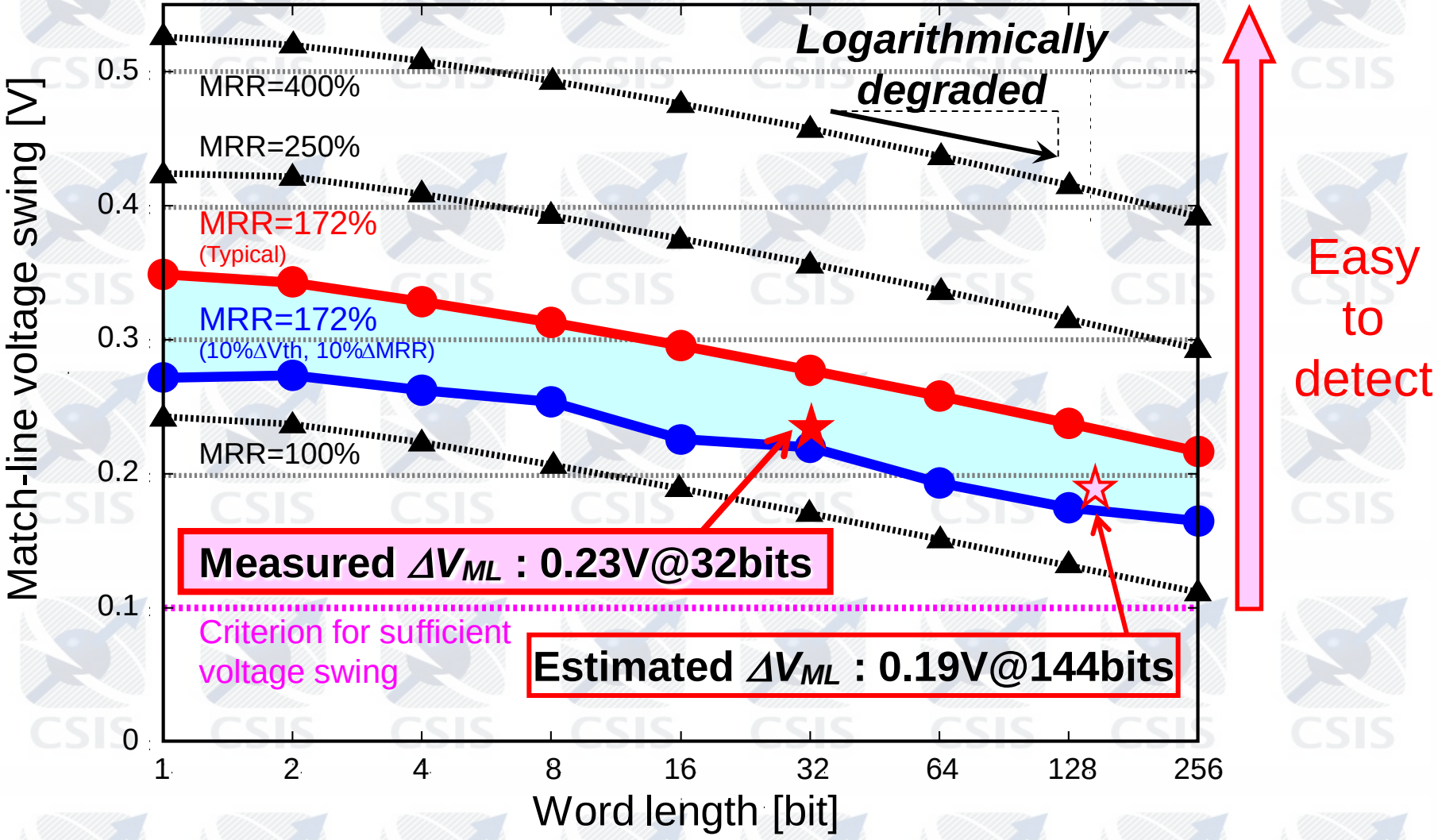
Fabricated NV-TCAM Test Chip





Process	90 nm 1P5M CMOS/MTJ
Cell structure	6T-2MTJ
MTJ size	100 nm x 200 nm
Cell size	10.35 μm^2
Array configuration	32bits x 64words
Match delay	0.29 ns
Supply voltage	1.2 V

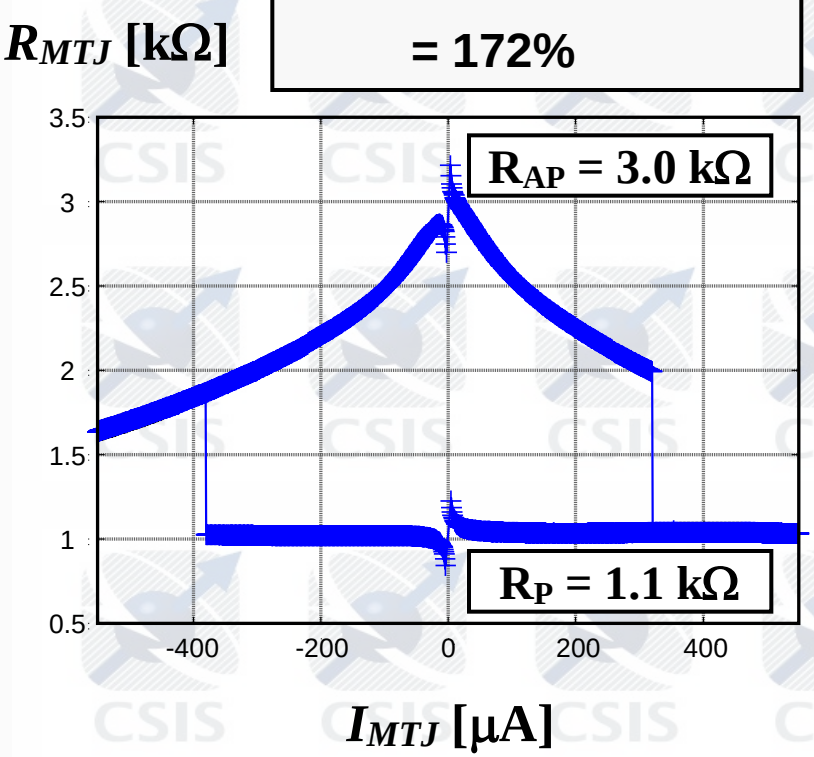
Match-Line Voltage Swings (Simulated and Measured)



Sufficient match-line voltage swing is obtained.

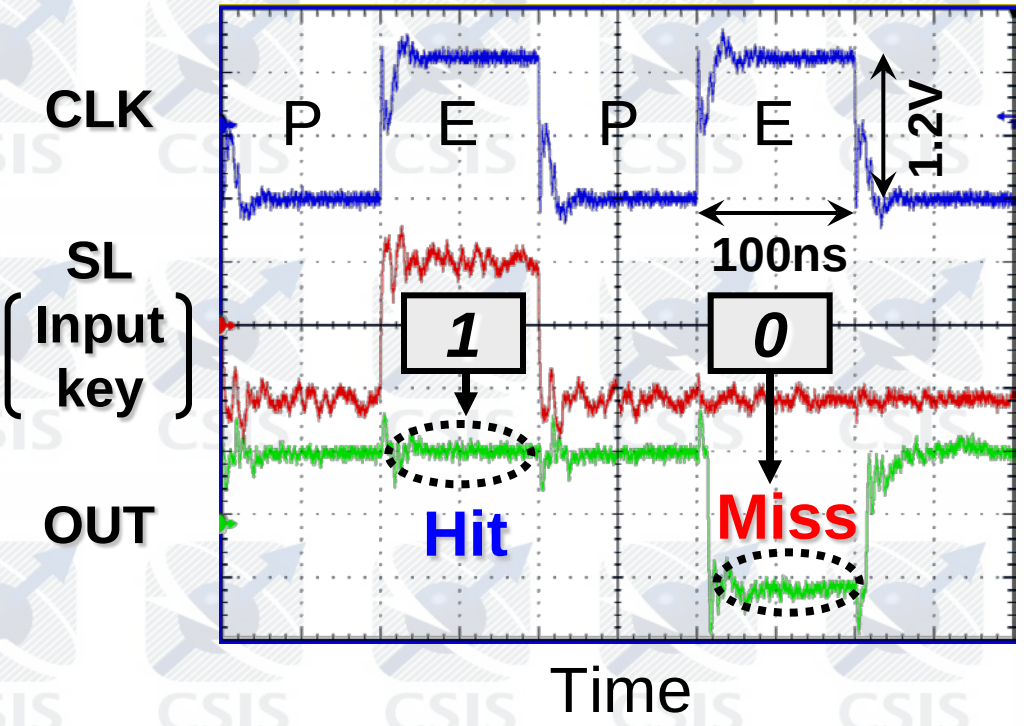
Chip Measurements

$$MRR = \frac{R_{AP} - R_P}{R_P} \times 100 = 172\%$$



P : Precharge
E : Evaluate

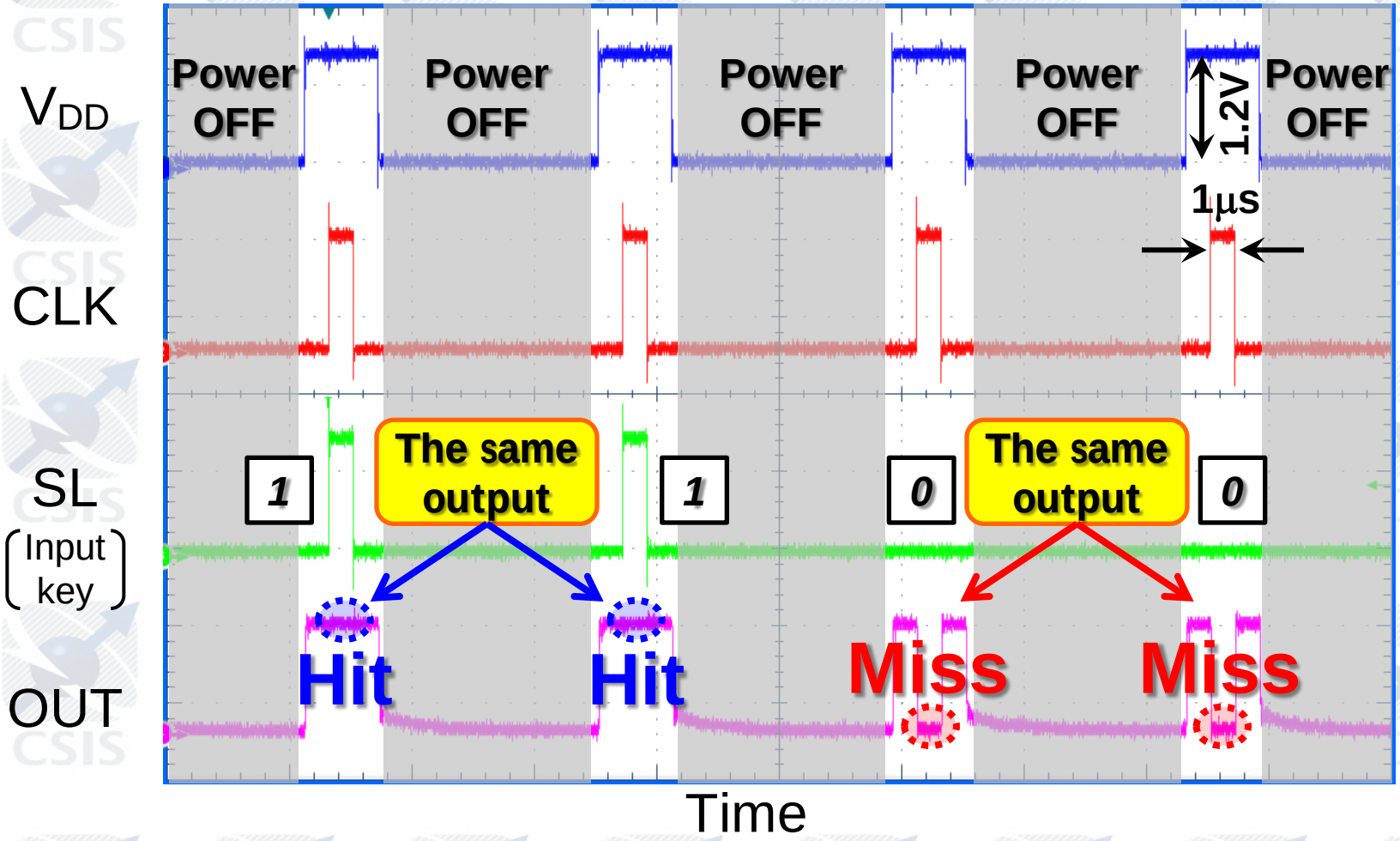
Voltages



Basic behaviors of the fabricated MTJ device and NV-TCAM have been successfully confirmed.

Measured Waveforms of Instant-ON/OFF

Voltages



Instant ON/OFF of the fabricated chip has been successfully confirmed.

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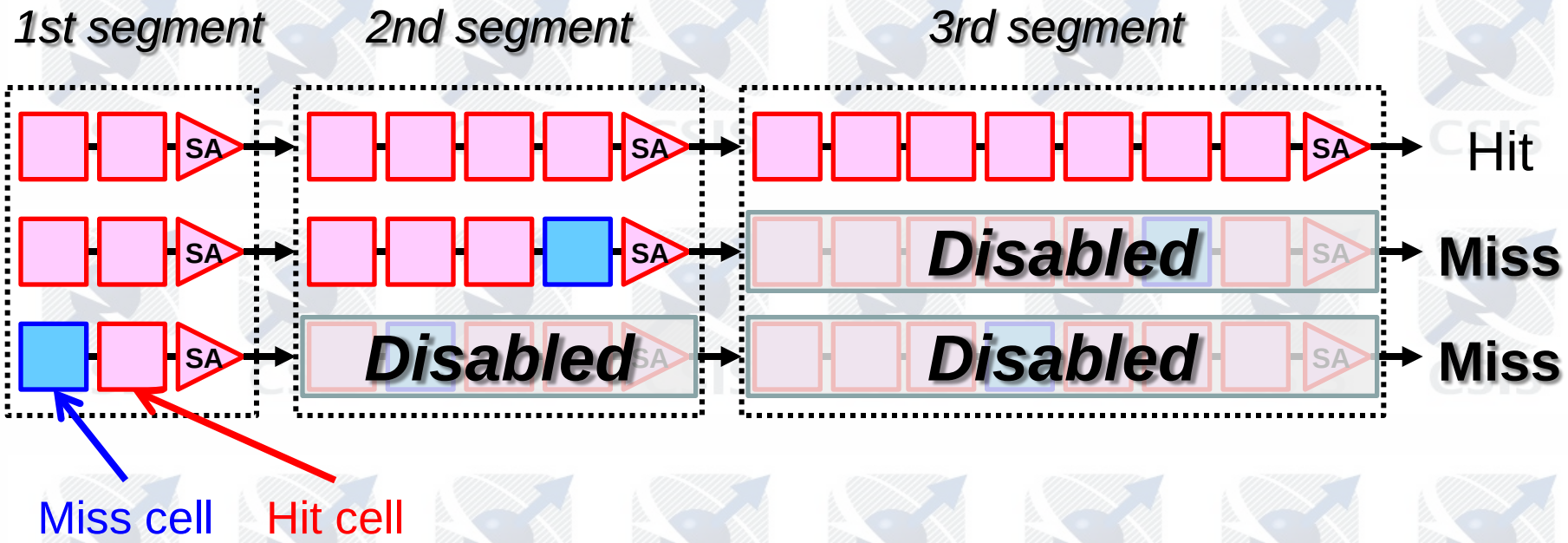
Approach for Low-Power NV-TCAM

Three-Level Segmented Match-Line Scheme



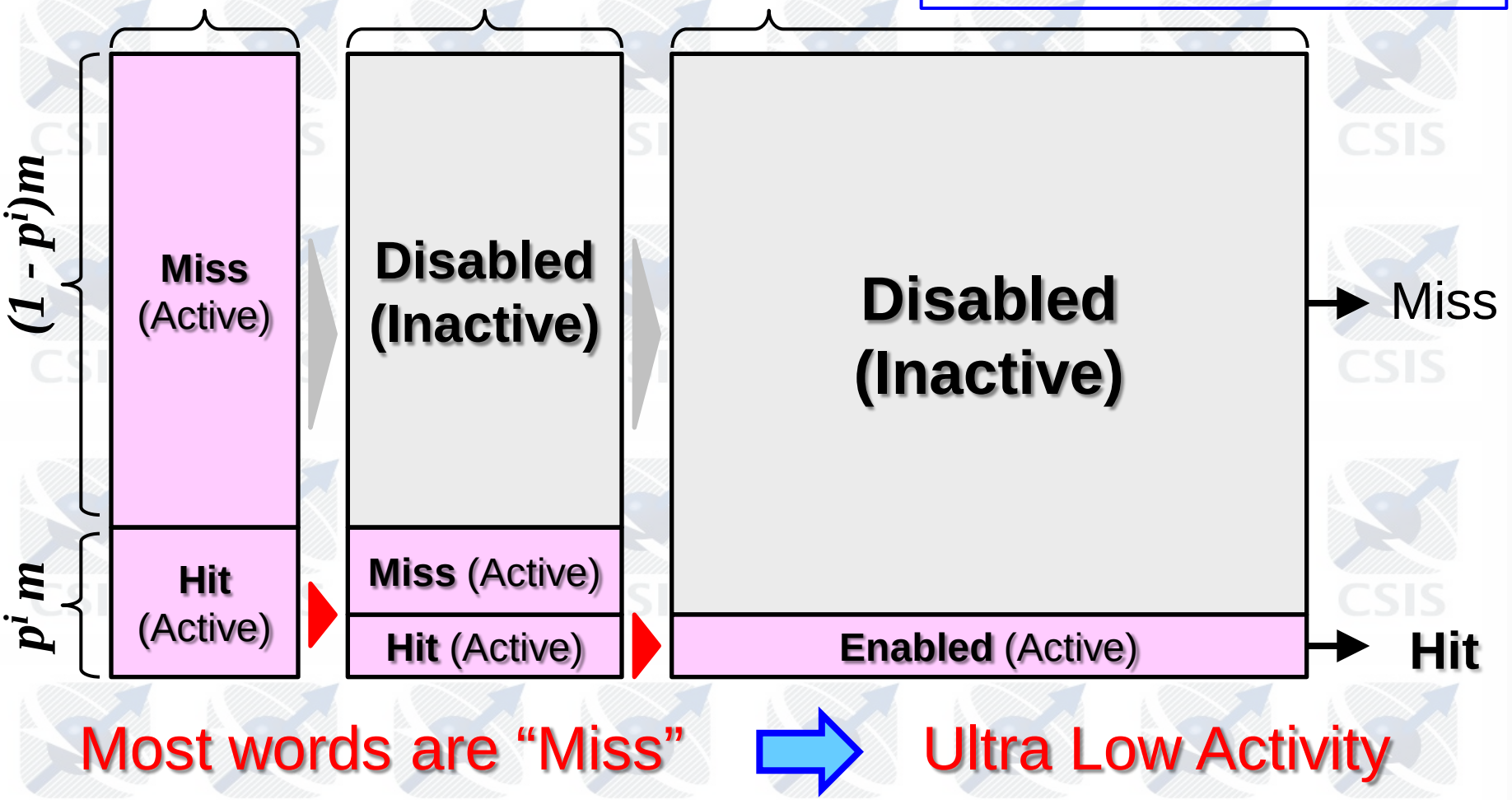
If current segment is “Miss,” then next segment is disabled.

Decreased activity rate ⇨ Low-Power

Image of Cell Array Activity

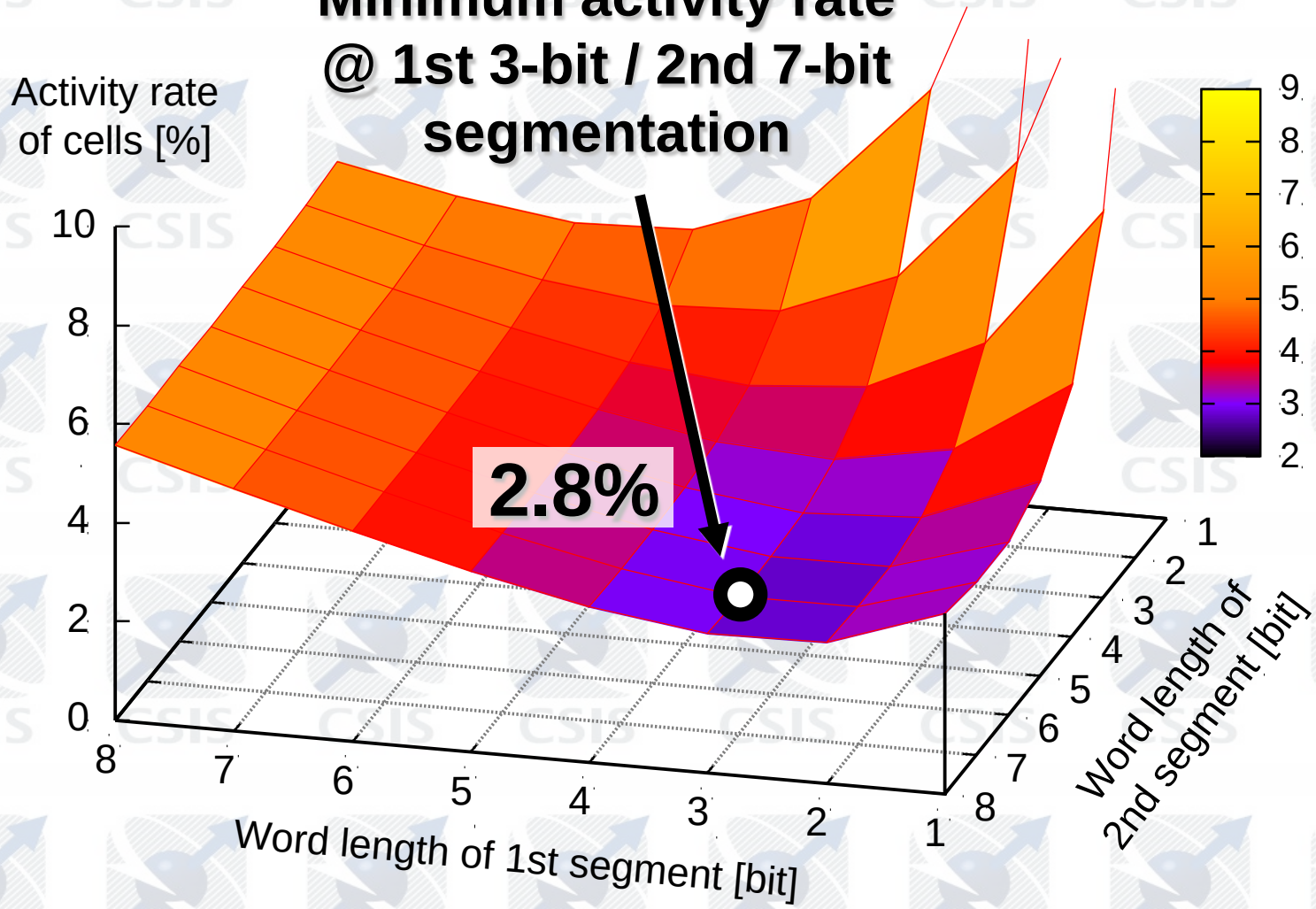
m-word x n-bit cell array

Hit probability of cell (p):
2/3 (using masked bit)
1/2 (not using masked bit)



Most words are "Miss" ⇨ Ultra Low Activity

Cell Activity Rate



Performance Evaluations

Array structure		144-bit x 256-word
Cell activity [%]		2.8
Search energy [fJ/bit/search]		1.04 (Comparable to CMOS-based TCAM within a few fJ/bit/search)
Standby power [W]	**Sleep mode**	**0 (@Power-OFF)**
	Search mode	**Negligible (@2.8% activity)**

HSPICE simulation under a 90nm CMOS technology @1.2V

Low-standby-power nonvolatile TCAM is successfully realized under comparable search energy with CMOS-based one.

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Conclusions

We have proposed and demonstrated 6T-2MTJ-based fully-parallel NV-TCAM.

Cell Circuit Techniques:

- Fewest transistor counts with nonvolatility
- Bit-parallel equality-search capability in a long word based on 1-transistor ML voltage keeper array

Word Circuit Techniques:

- Eliminate wasted cell activation based on three-level segmented match-line scheme

→ Negligible standby power under comparable search energy with CMOS-based TCAM