5th international Conference on Superconductivity and Magnetism
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Spintronics Nano-Devices for VLSIs

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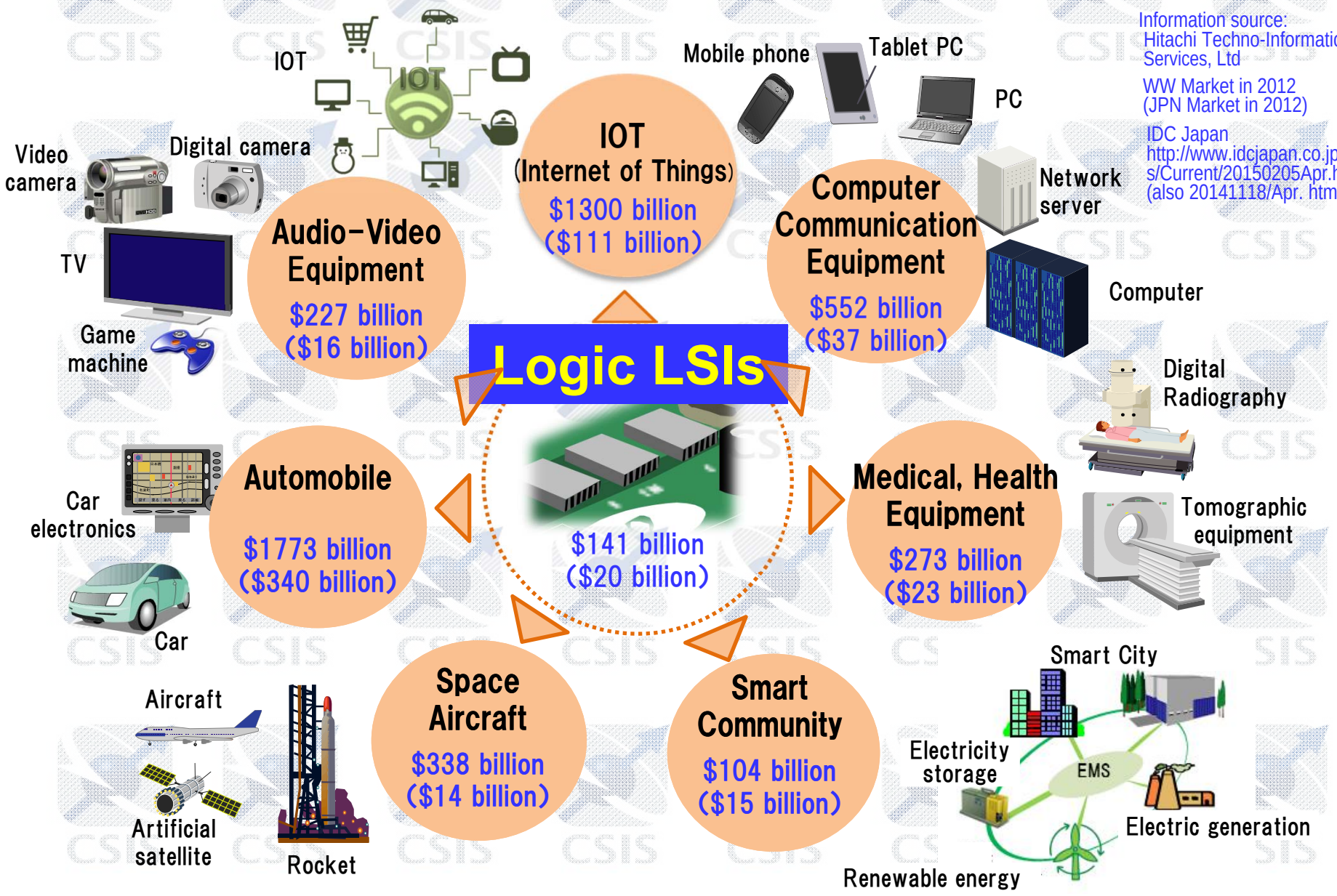
and by the R & D for Next-Generation Information Technology of MEXT

http://www.csis.tohoku.ac.jp/

Logic VLSIs



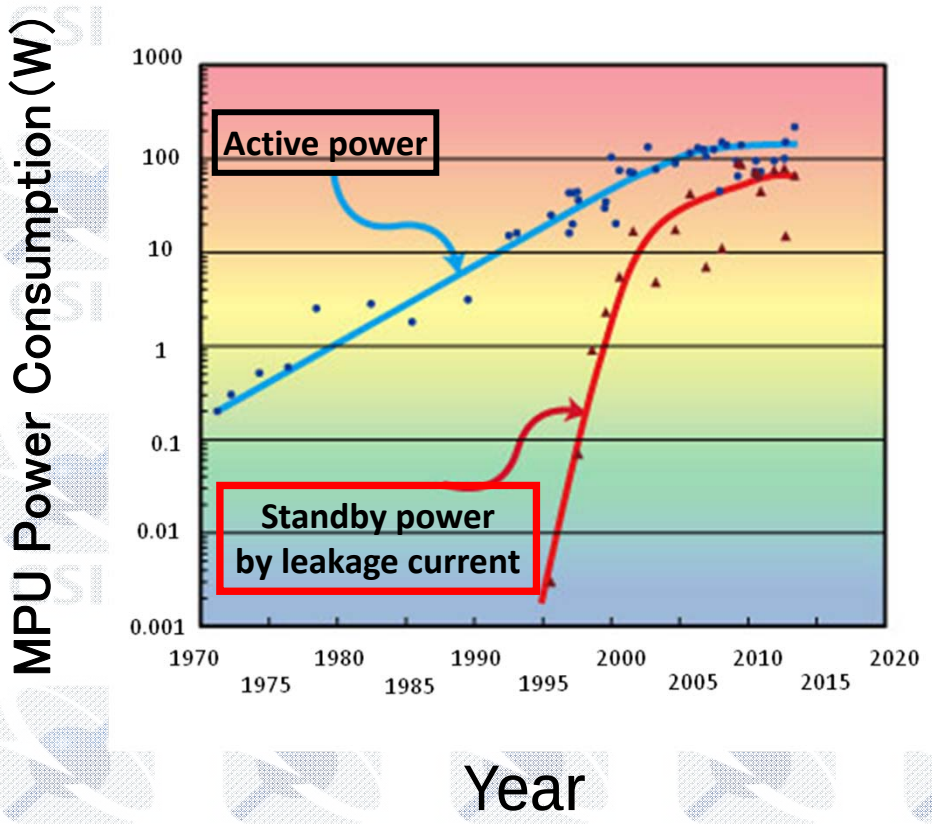
Information source:
Hitachi Techno-Information Services, Ltd

WW Market in 2012
(JPN Market in 2012)

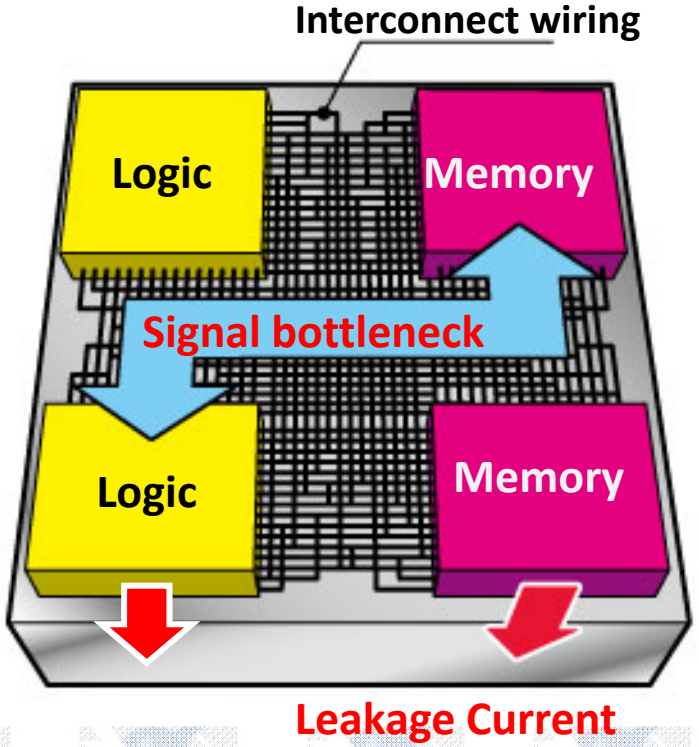
IDC Japan
http://www.idcjapan.co.jp/Press/Current/20150205Apr.html
(also 20141118/Apr. html)

Challenges VLSI Technology Face

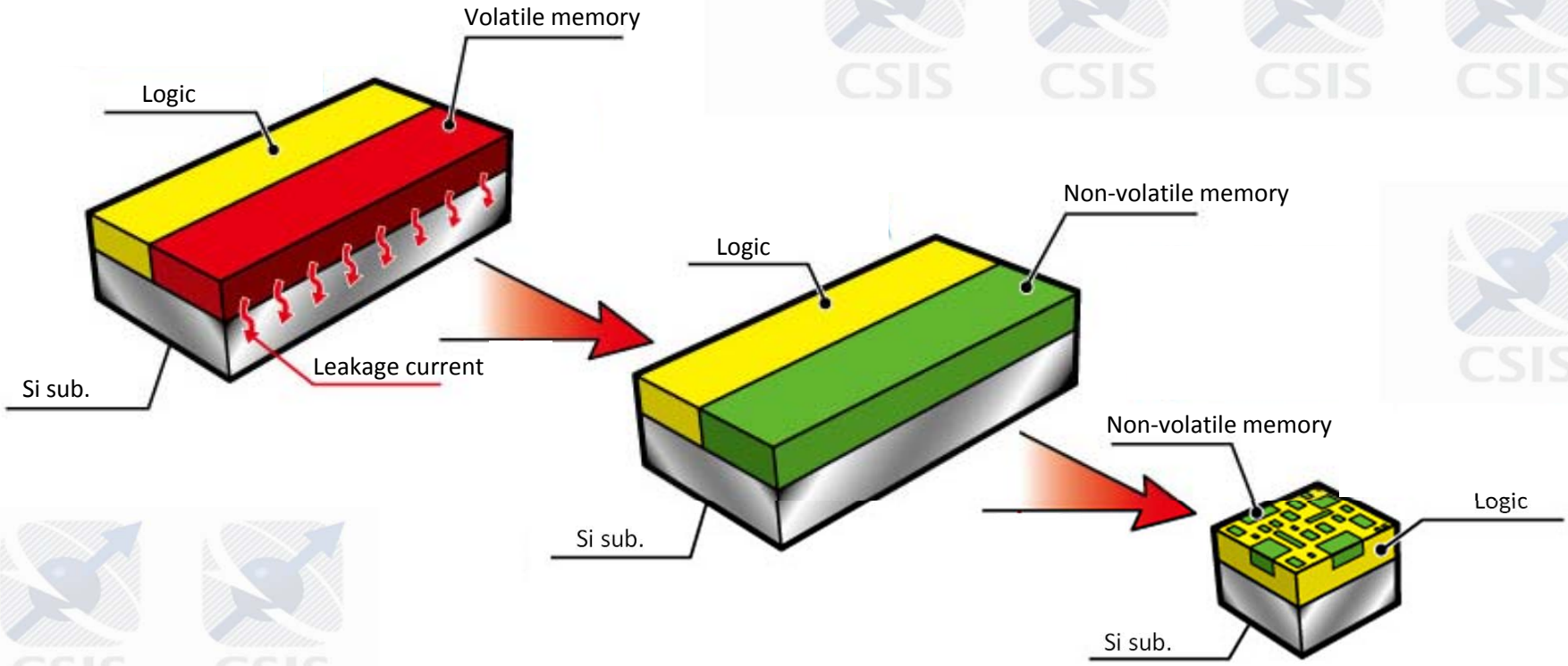
Power Consumption



Interconnection Delay



Toward Nonvolatile CMOS VLSI

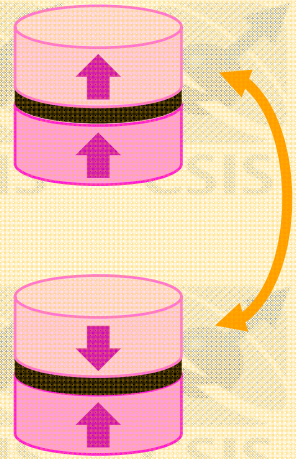


Nonvolatile Memories

Features of non-volatile for memory device	Flash	FRAM	Spin Device
Access Speed	△	○	○
Non destructive Read	○	△	○
Write Endurance	×	△	○
Scalability	○	△	○
Operation Voltage	×	△	○

Magnetic Tunnel Junction (MTJ)

Low resistance “0”



High resistance “1”

Nonvolatile Memories

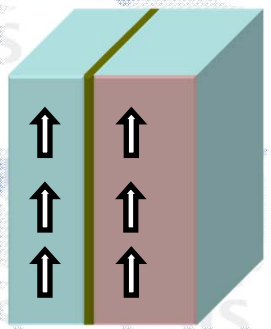
Comparison: ReRAM, PCRAM, and STT-MRAM (Spin)

	ReRAM	PCRAM	STT-MRAM
Program Current	10^{-4}A	10^{-4}A	10^{-5}A
Program Time	50ns	100ns	0.5ns-10ns
Read Time	< 5ns	< 5ns	< 5ns
Retention	10yrs	10yrs	10yrs
Endurance	10^{6}	10^{9} - 10^{12}	10^{15}

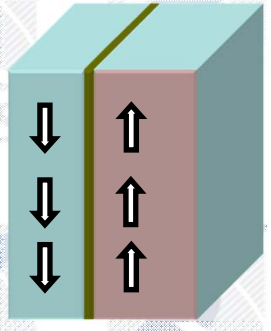
Magnetic Tunnel Junction

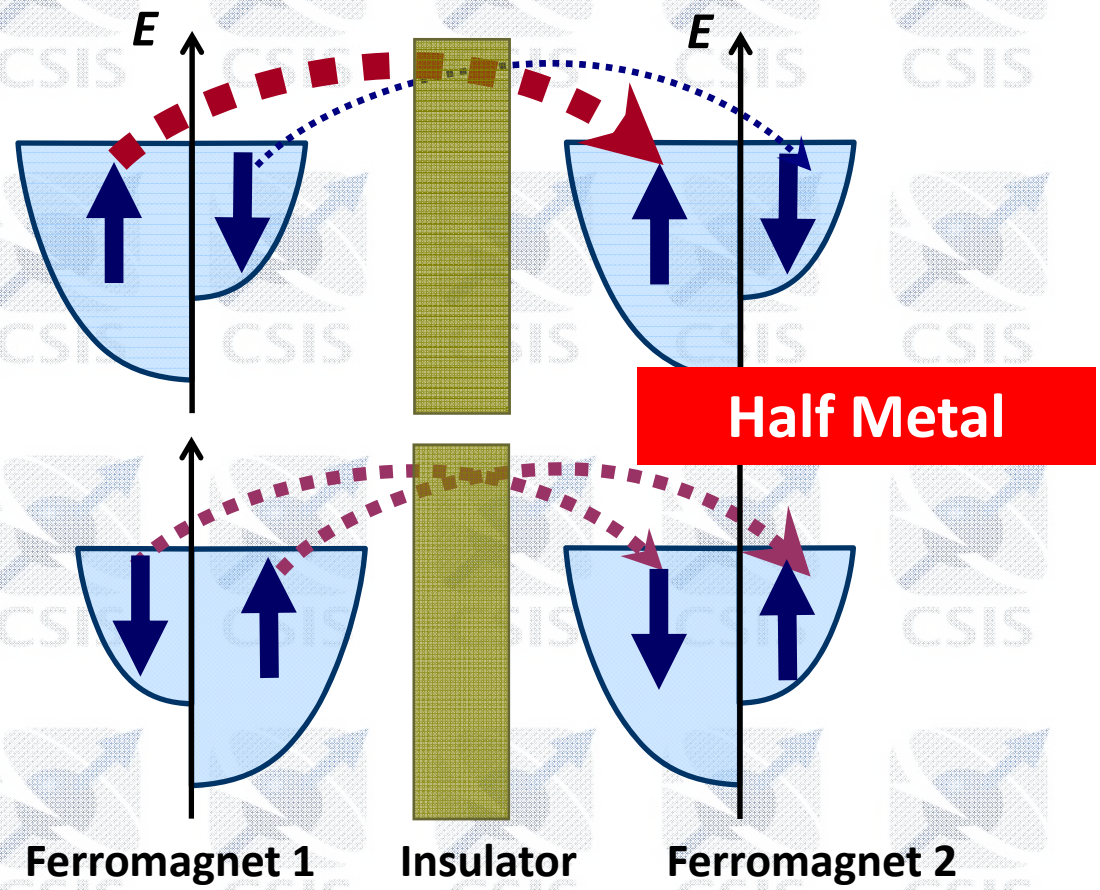
$$\text{Tunnel MagnetoResistance (TMR)} = \frac{R_{AP} - R_P}{R_P} = \frac{2P^2}{1-P^2}$$

Parallel



Antiparallel



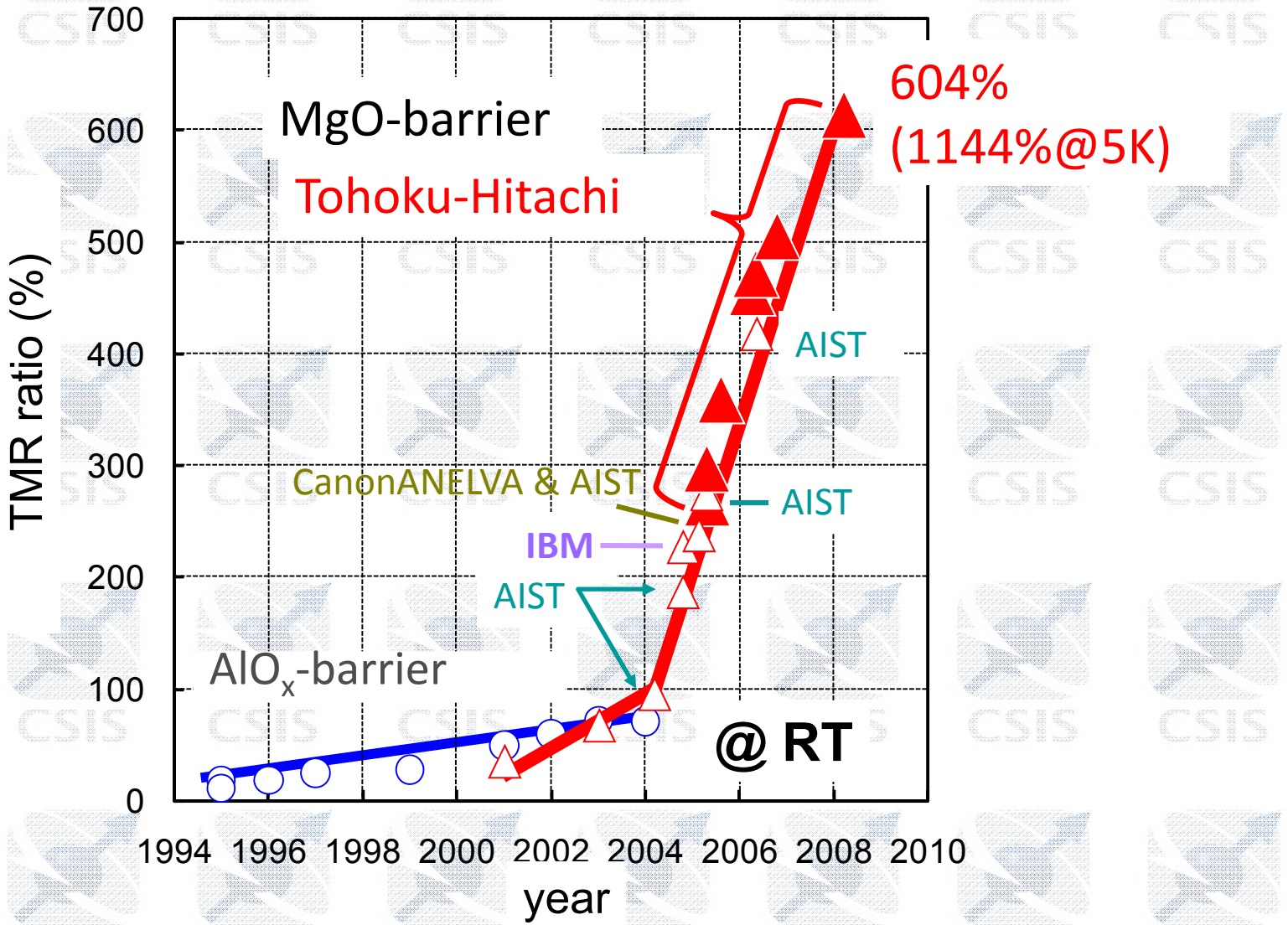


Room temperature TMR: Miyazaki and Tezuka (Tohoku U.), *J. Mag. Mag. Mat.* 1995 and Moodera *et al. Phys. Rev. Lett.* 1995.

Required Properties

- High tunnel magnetoresistance ratio > 100%
- High thermal stability $\Delta = E/k_BT > 60$
- Unlimited endurance
- Low switching current
- High speed read and write
- High temperature tolerance ~ 400 °C
- Scalability 40 nm → 20 nm → 10 nm

TMR ratio of MTJs



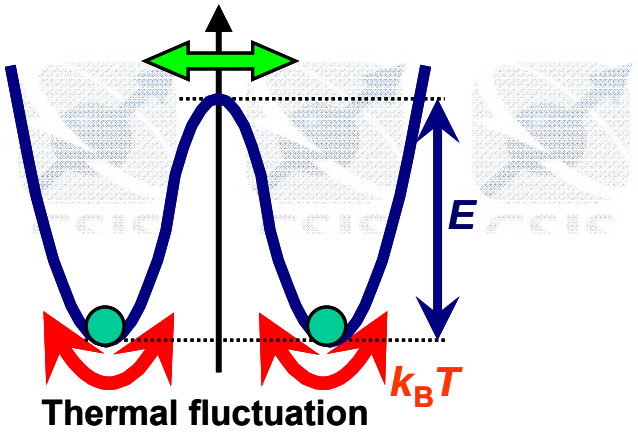
I_{c0} and $\Delta = E/k_B T$

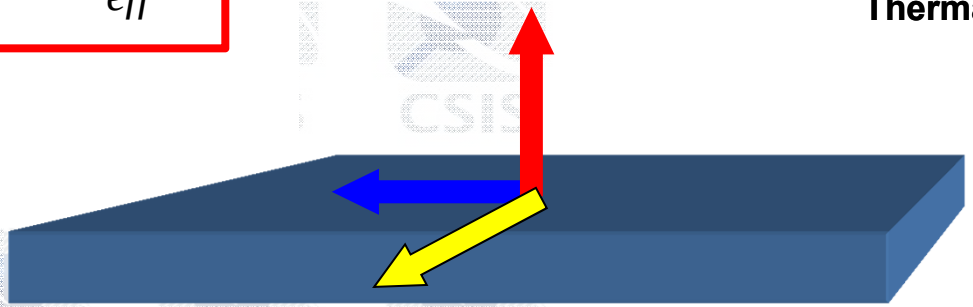
in-plane

$$E = K_{eff} V$$

$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g}\left(K_{eff}^{*} V\right)$$

$$K_{eff}^{*} \square K_{eff}$$





I_{c0} and $\Delta = E/k_B T$

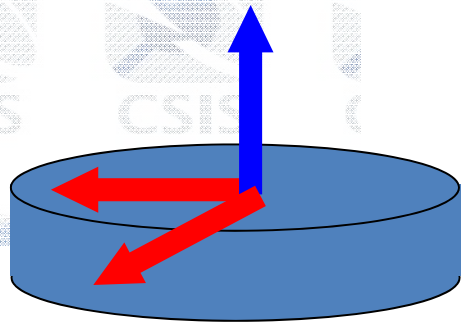
perpendicular

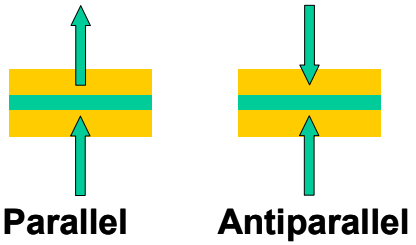
$$E = K_{eff} V$$

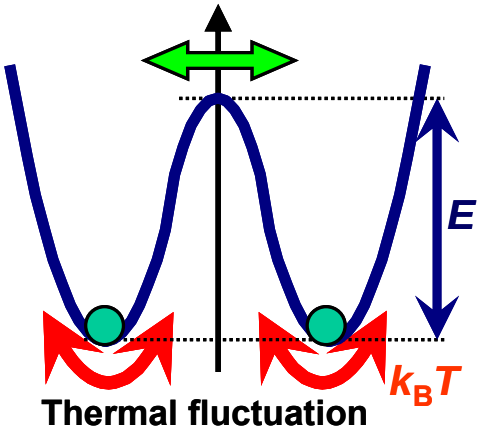
$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g}\left(K_{eff} V\right)$$

$$\propto \alpha E$$

$$K_{eff} = K_{eff}$$







Comparison of MTJs (early 2010)

Type	Stack structure (nm)	Size (nm)	MR (%)	RA ($\Omega\mu m^2$)	J_{C0} (MA/cm^2)	I_{C0} (μA)	$\Delta=E/k_BT$	I_{C0}/Δ	T_a (°C)	Ref.
i-MTJ	CoFeB(2)/Ru(0.65)/CoFeB(1.8) SyF	100x200	>130	~10	2	~400	65	~6.2	300-350	J. Hayakawa et al., IEEE T-Magn., 44, 1962 (2008)
p-MTJ	L10-FePt/MgO(0.4)/MgO(1.0)/L10-FePt(t)	Blanket	120 (CIPT)	11.8k	-	-	-	-	500	M. Yoshizawa et al., IEEE T-Magn., 44, 2573 (2008)
p-MTJ	L10-FePt/MgO(0.5)/CoFeB/Co based superlattice	Blanket	(CIPT)		-	-	-	-	-	H. Yoda et al., Magnetics Jpn. 5, 184 (2010) [in Japanese].
p-MTJ	[Co/Pt]/CoFeB/CoFeO/CoFeB/TbFeCo	Blanket	(CIPT)	4.4-10	-	-	-	-	225	K. Yakushiji et al., APEX 3, 053033 (2010)
p-MTJ	[CoFe/Pd]/CoFeB/MgO/CoFeB/[CoFe/Pd]	800x800 N	100 (113)	18.7k (20.2k)	-	-	-	-	350 (325)	K. Mizunuma et al., MMM&INTERMAG2010
p-MTJ	CoFeB (t) TbFeCo (5)	130 φ	~15		4.7	650	107	6.08	-	M. Nakayama et al., APL 103, 07A710 (2008)
p-MTJ	L1$_0$ alloy	50-55 φ	-	-	-	49	56	0.88	-	T. Kishi et al., IEDM 2008
p-MTJ	Fe-based L1$_0$ (2)/CoFeB (0.5)	-	-	-	-	9	-	-	-	H.Yoda et al., Magnetics Jpn. 5, 184 (2010) [in Japanese].

FePt

FePt & Co-based SL

Co/Pt & TbFeCo

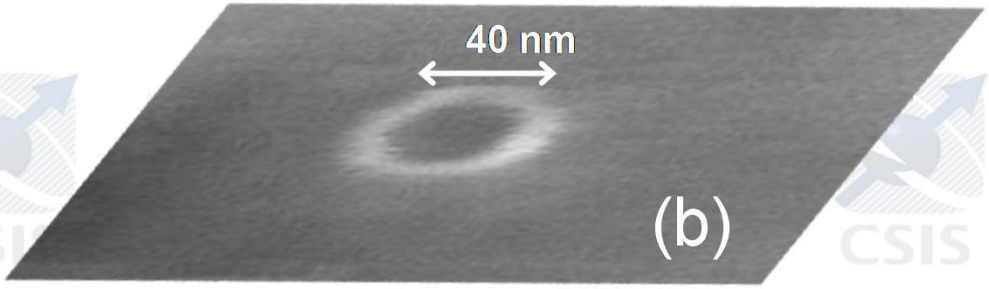
CoFe/Pd

TbFeCo

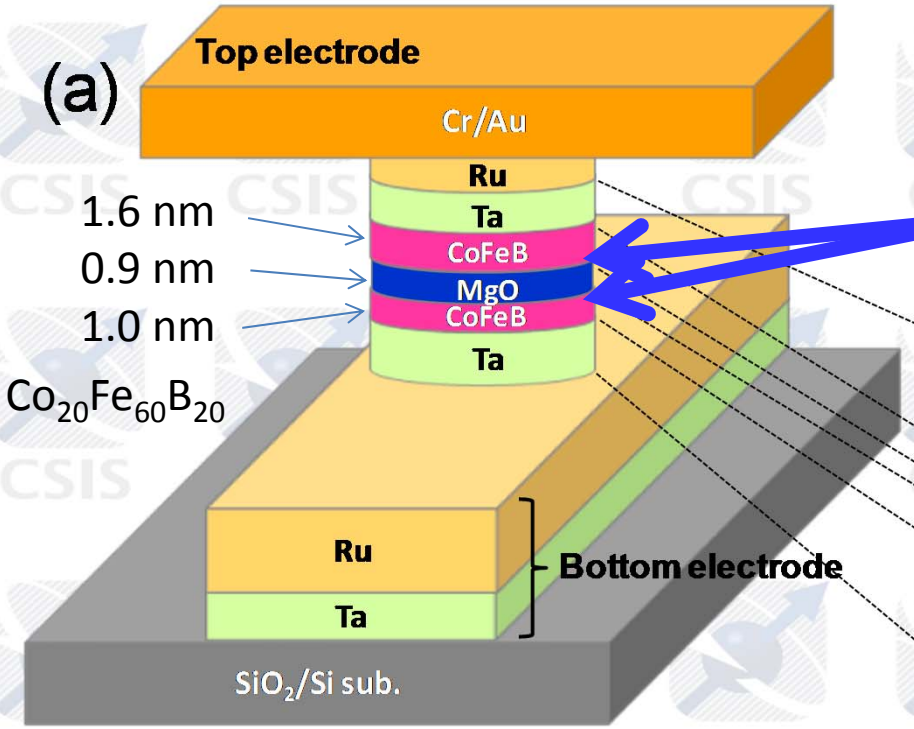
L1$_0$ alloy

Fe-based L1$_0$

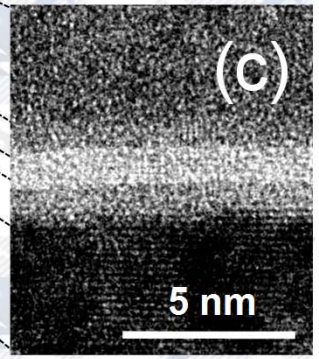
Perpendicular MgO-CoFeB MTJ



J_{C0} = 3.8 MA/cm^2
(I_{C0} = 48 μA)
E/k_BT ~ 40
TMR ratio = 110%
T_a = 350°C

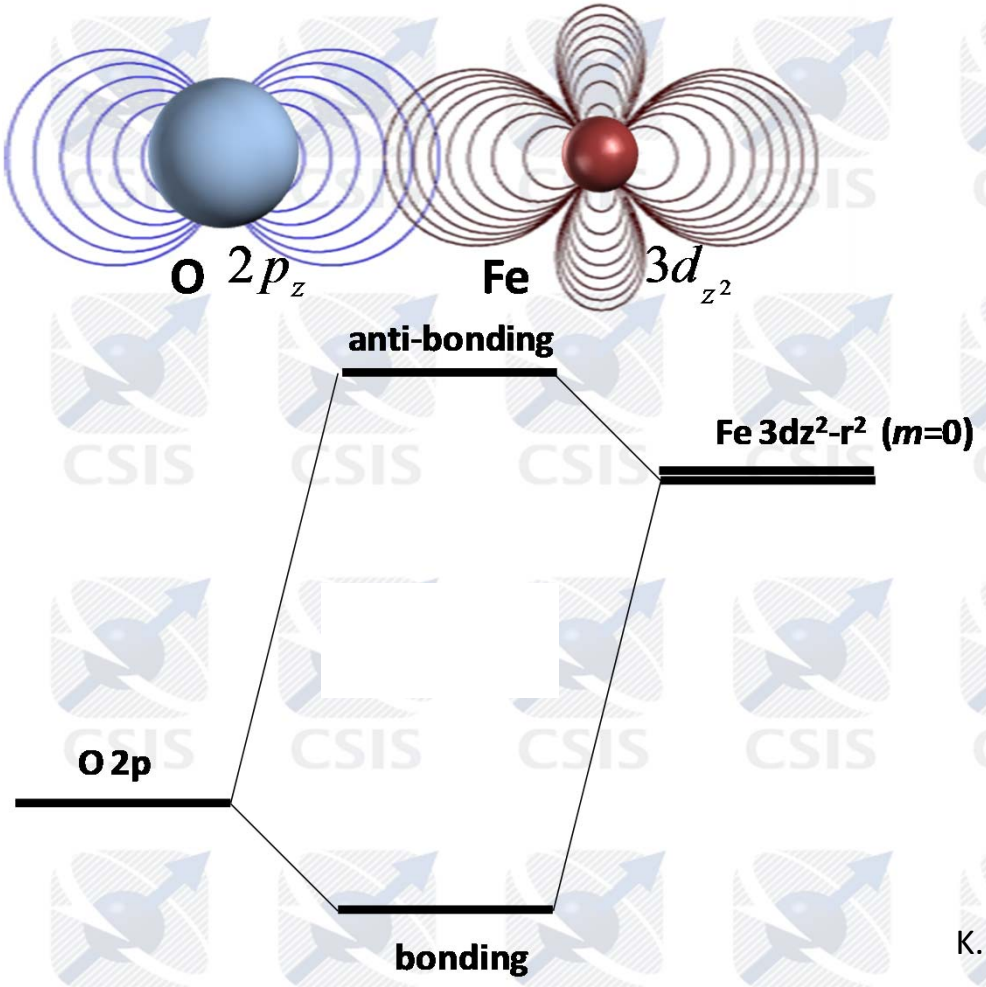


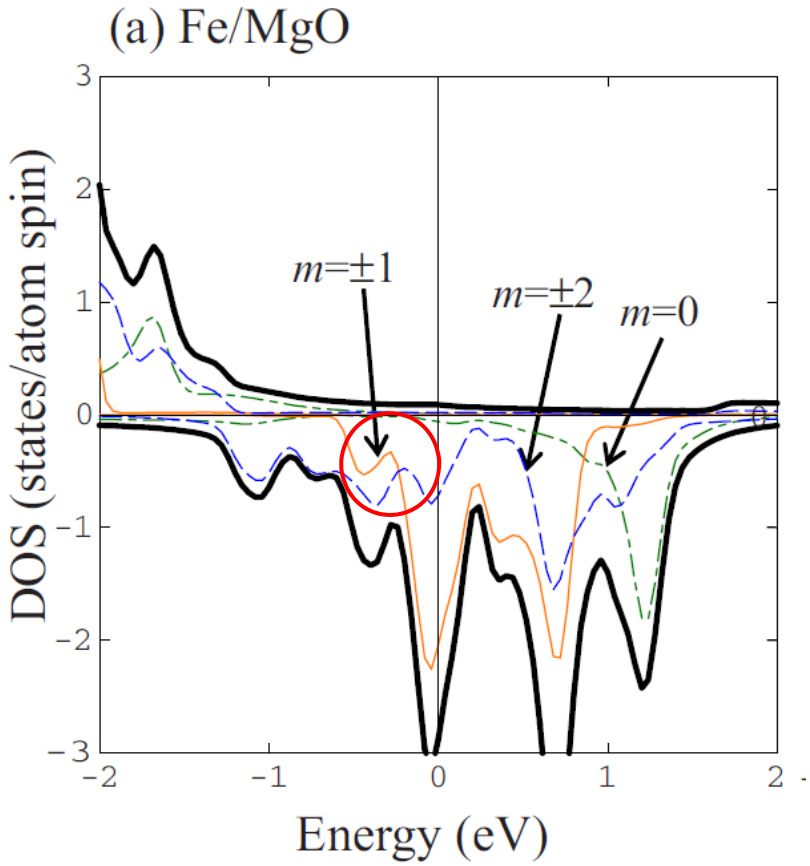
interface perpendicular anisotropy



S. Ikeda *et al.*, Nature Mat. **9**, 721 (2010)

Perpendicular anisotropy at the CoFeB/MgO interface





K. Nakamura *et al.*, Phys. Rev. B, 81, 220409(R) (2010)

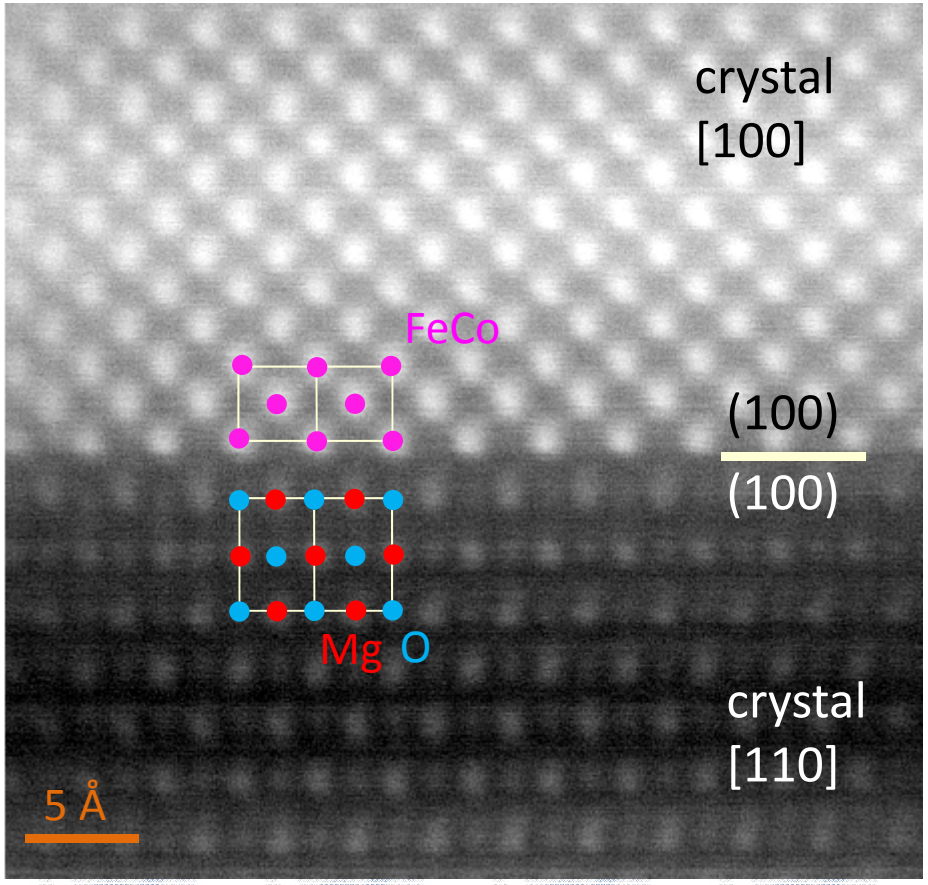
Co-Fe atoms on O sites in MgO

MgO-Fe system

- High TMR ratio and interfacial anisotropy are predicted by first-principles calculation.

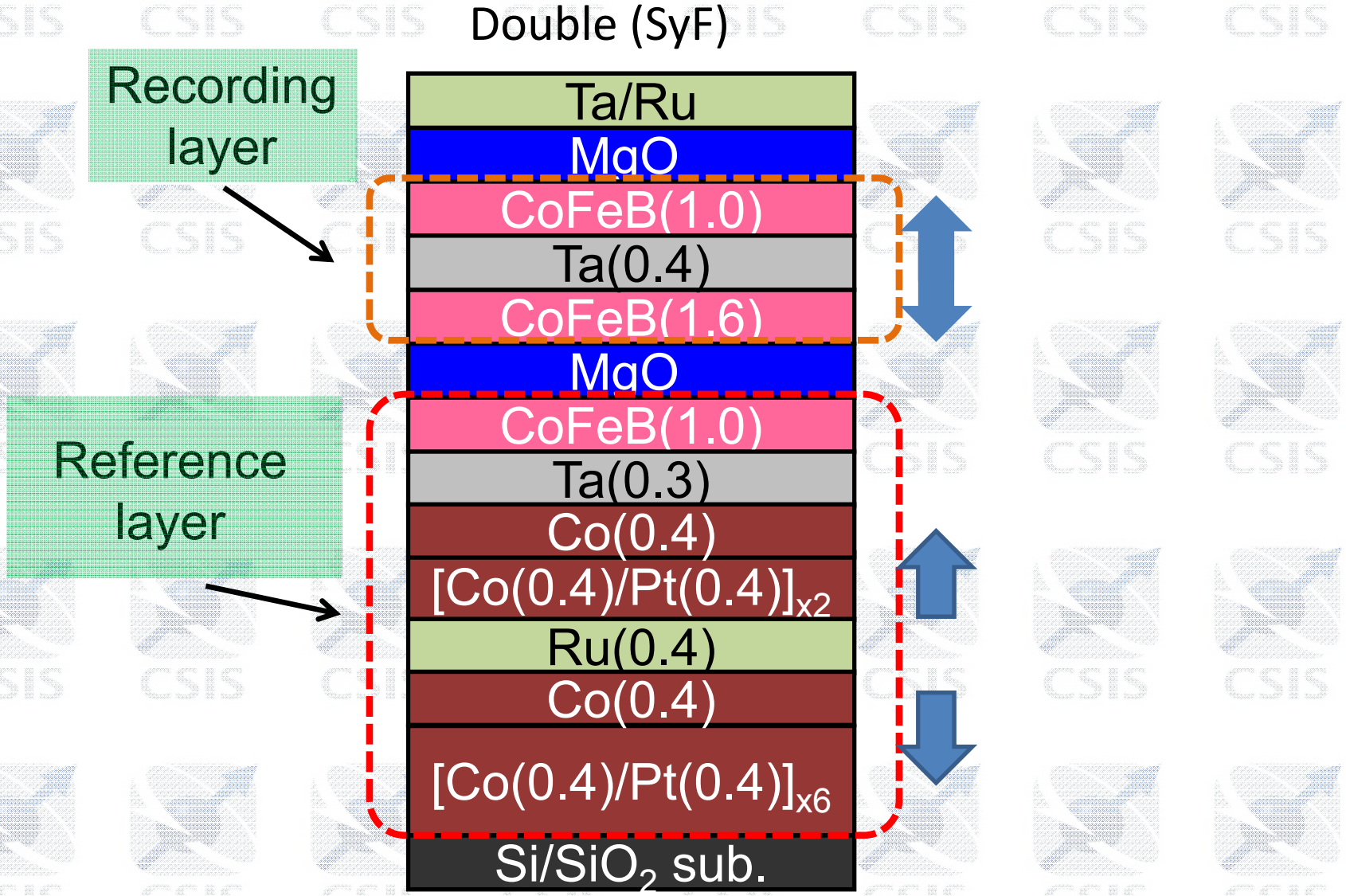
W. H. Butler *et al.*, Phys. Rev. B **63**, 054416 (2001).
J. Mathon *et al.*, Phys. Rev. B **63**, 220403 (2001).
K. Nakamura *et al.*, Phys. Rev. Lett. **102**, 187201 (2009).

Structural analysis for high performance CoFeB-MgO MTJ stack confirmed that Fe(Co) atoms sit on top of O atoms



Collaborative work with Prof. Ikuhara-Lab., Nano Lett. **16**, 1530 (2016).

Device structure (full stack)



H. Sato *et al*., Appl. Phys. Lett. **101**, 022414 (2012), IEDM 2013, p. 3.2.1., Appl. Phys. Lett. **105**, 062403 (2014).

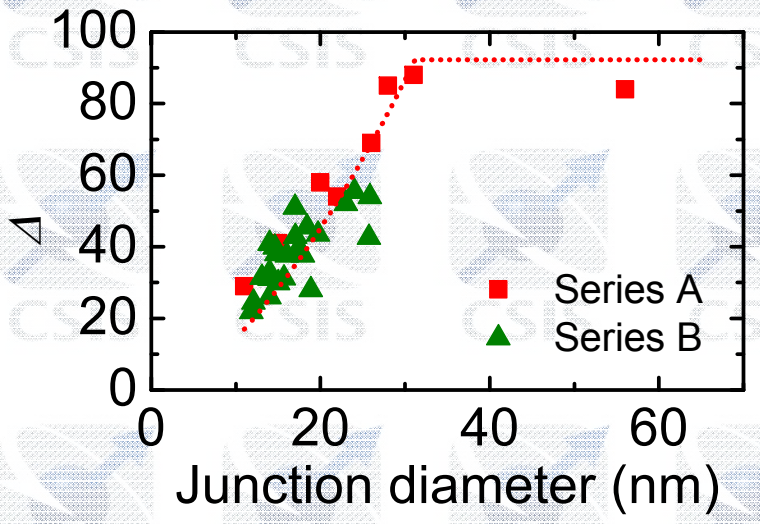
$\Delta = E/k_B T$, I_{C0} and efficiency

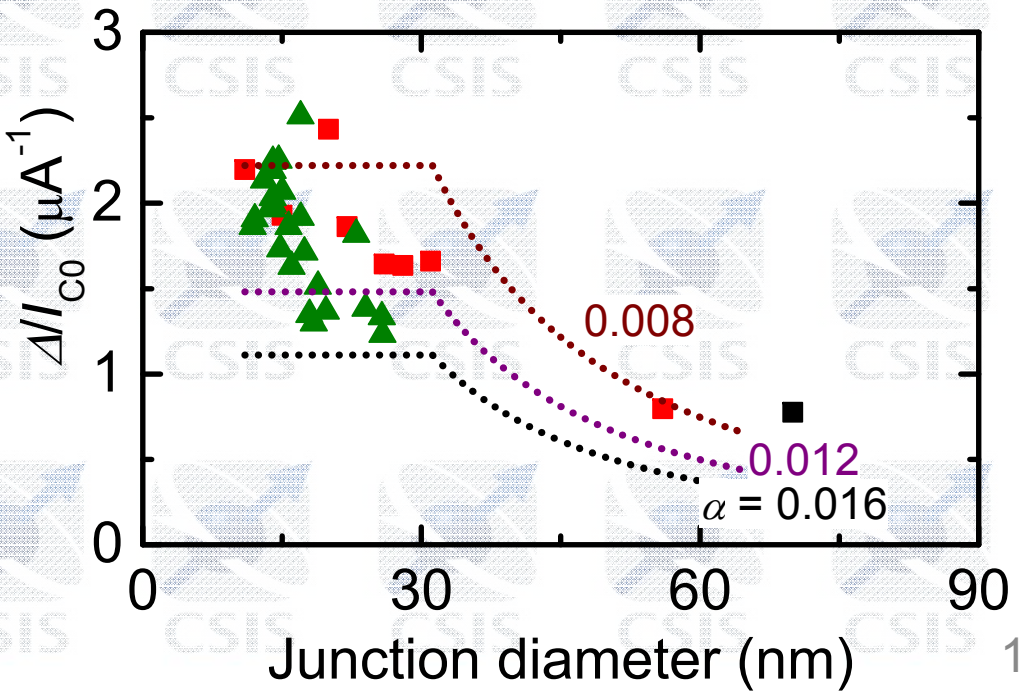
Perpendicular MTJ

$$E = \left(\frac{1}{2} M_S H_K\right) V = K_{eff} V$$

$$I_{C0} = \frac{2\alpha\gamma e}{\mu_B g(\theta)} \left(K_{eff} V\right)$$

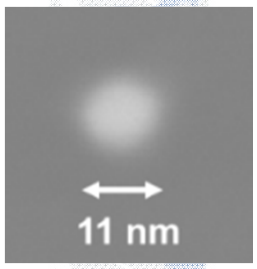
$$\propto \frac{\alpha}{g(\theta)} E$$

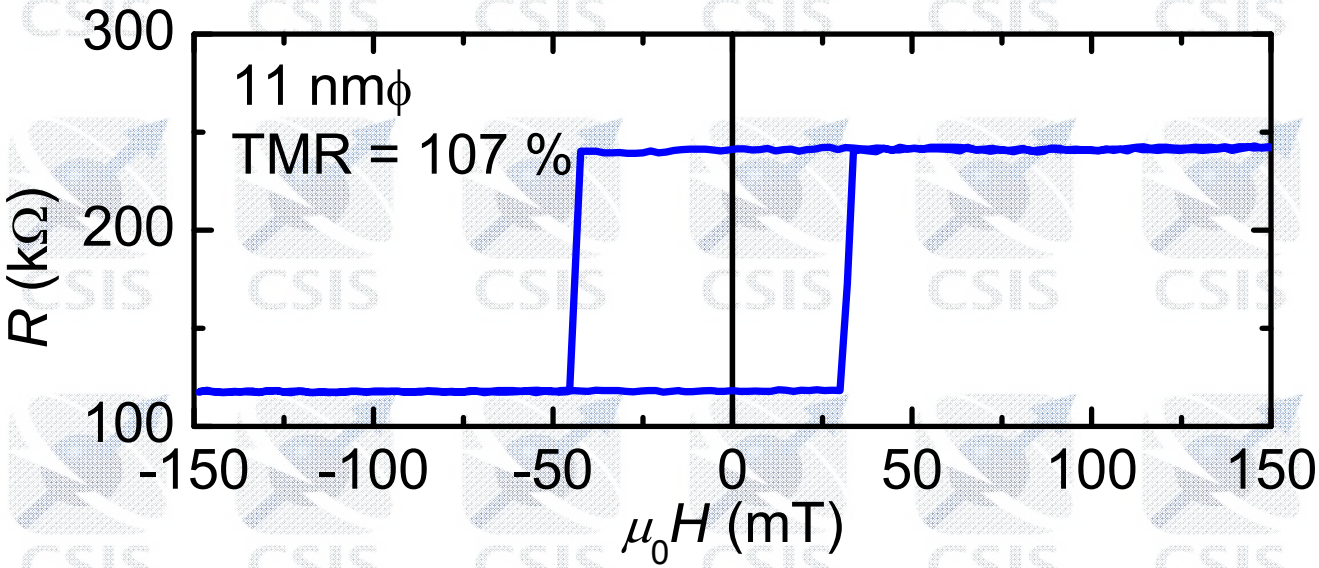


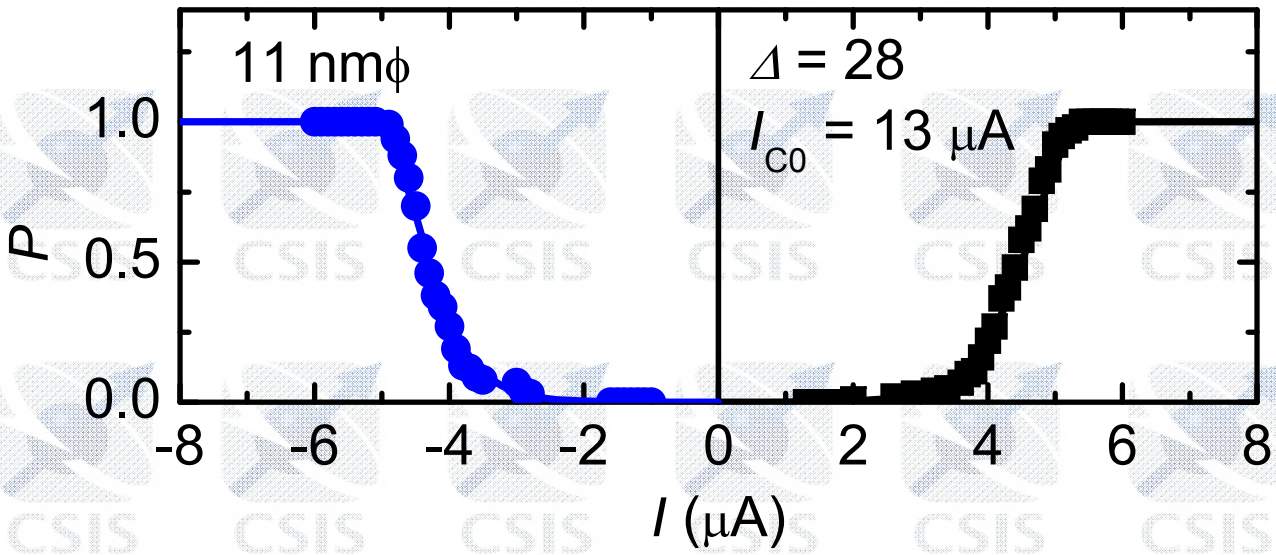


H. Sato *et al.*, Appl. Phys. Lett. **101**, 022414 (2012).
H. Sato *et al.*, IEDM 2013, p. 3.2.1.
H. Sato *et al.* Appl. Phys. Lett. **105**, 062403 (2014).

11 nmϕ MTJ (smallest MTJ)

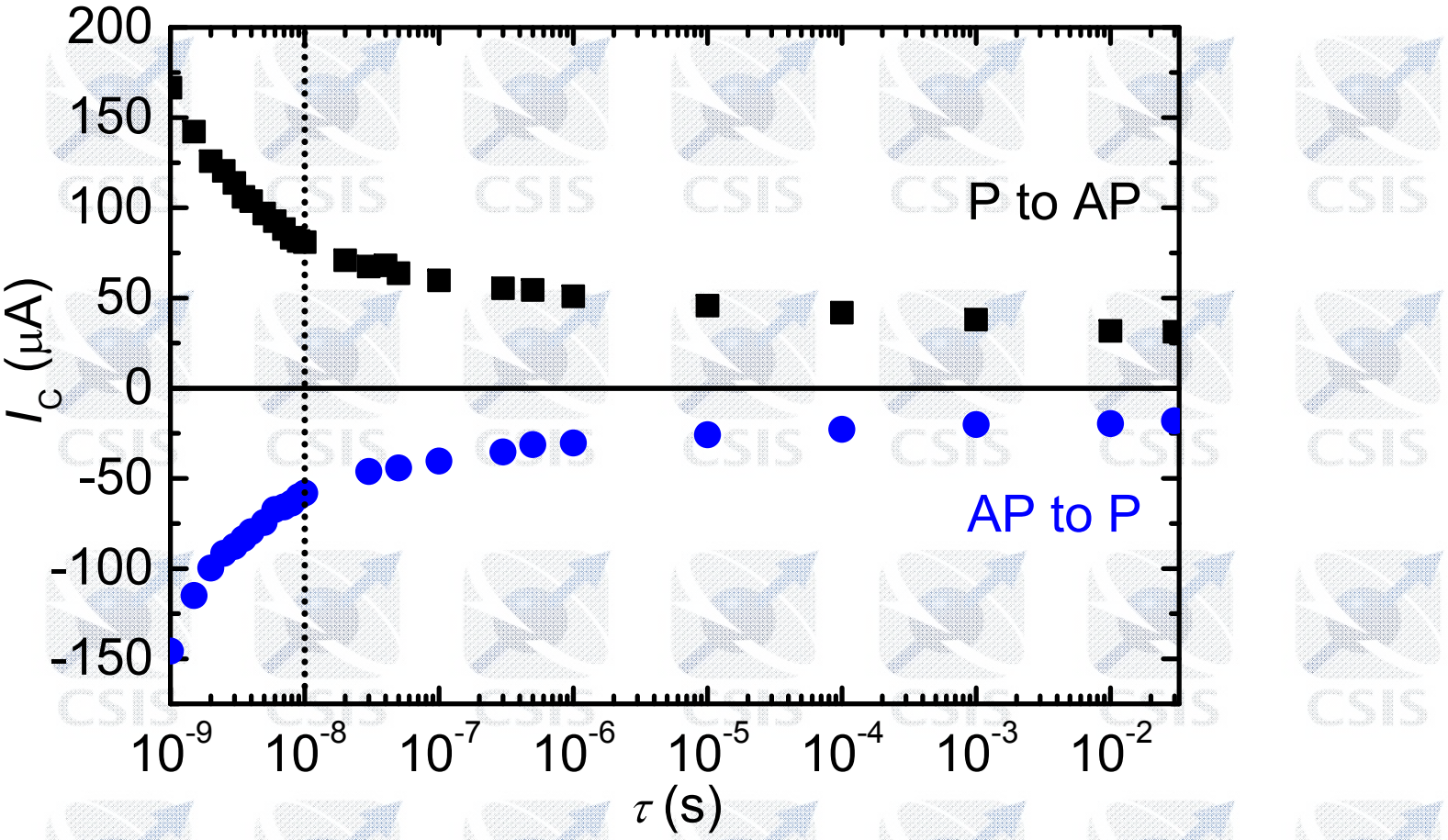




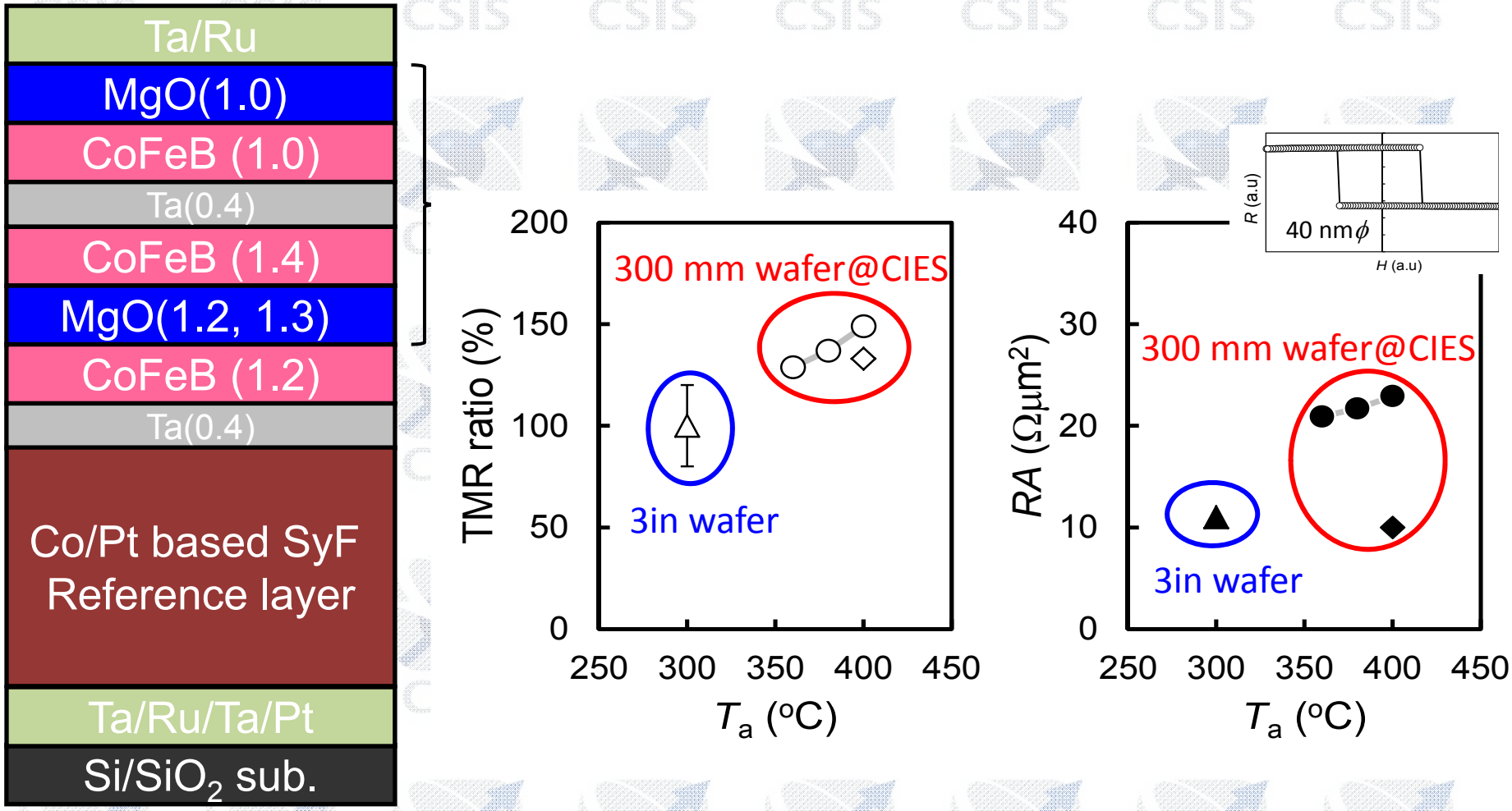


H. Sato *et al.* Appl. Phys. Lett. **105**, 062403 (2014).

Switching current versus switching time



MTJ stack on 300mm wafers



300 mm wafer
T_a = 360-400°C for 1hr

S. Ikeda, *et al*. IEDM2014

Required Properties

- High tunnel magnetoresistance ratio > 100%
- High thermal stability $\Delta = E/k_B T > 60$
- Unlimited endurance
- Low switching current
- High speed read and write
- High temperature tolerance ~ 400 °C
- Scalability 40 nm → 20 nm → 10 nm

Required Properties

- ✓ High tunnel magnetoresistance ratio > 100%
- ✓ High thermal stability $\Delta = E/k_BT > 60$
- ✓ Unlimited endurance
- ✓ Low switching current
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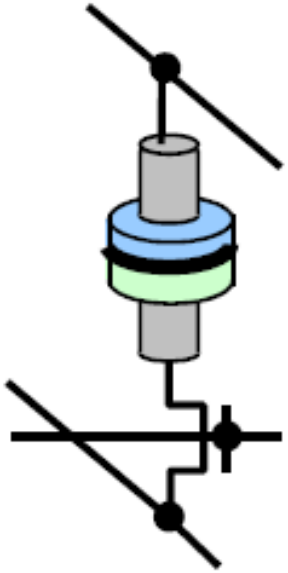
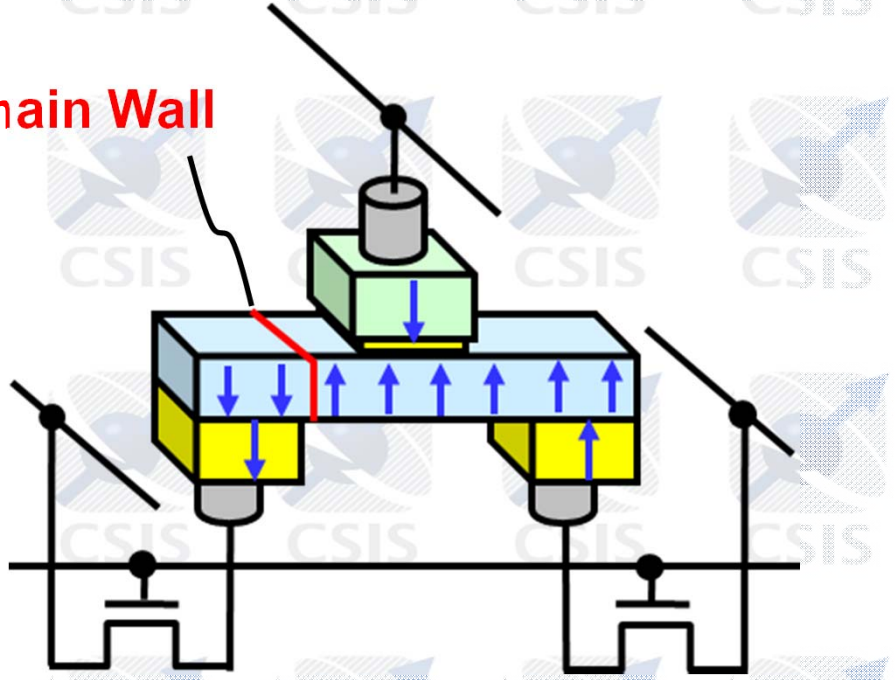
- ✓ High temperature tolerance ~ 400 °C
- ✓ Scalability 40 nm → 20 nm

Two and three terminal devices



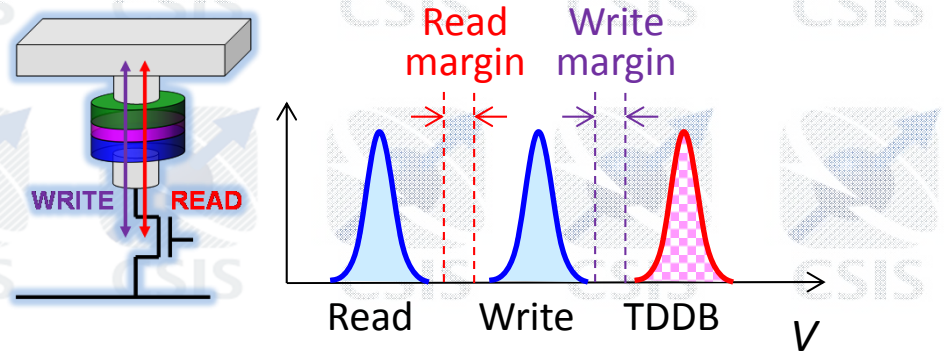


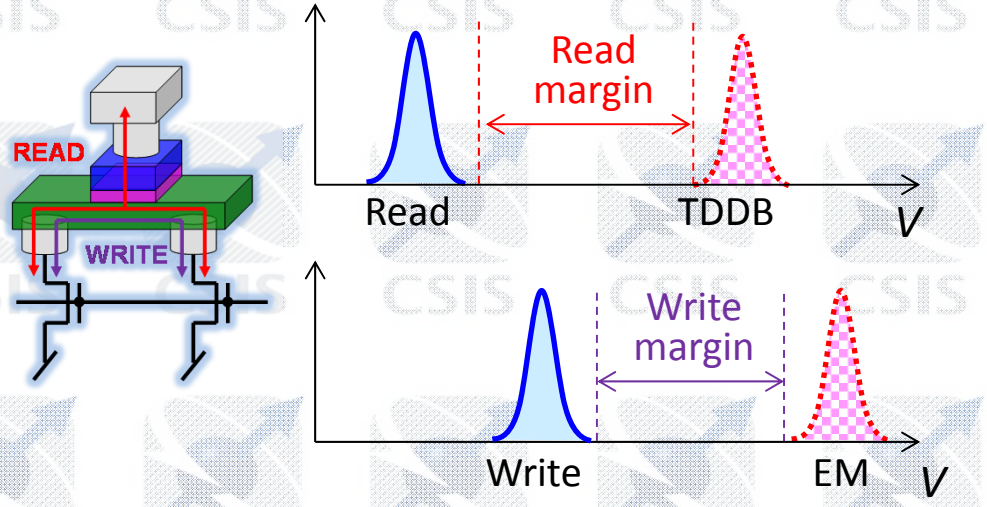
two terminal
(spin-transfer torque)
(electric-field)

three terminal
(domain wall)
(spin-orbit torque)

Nonvolatile, fast, low voltage and high endurance

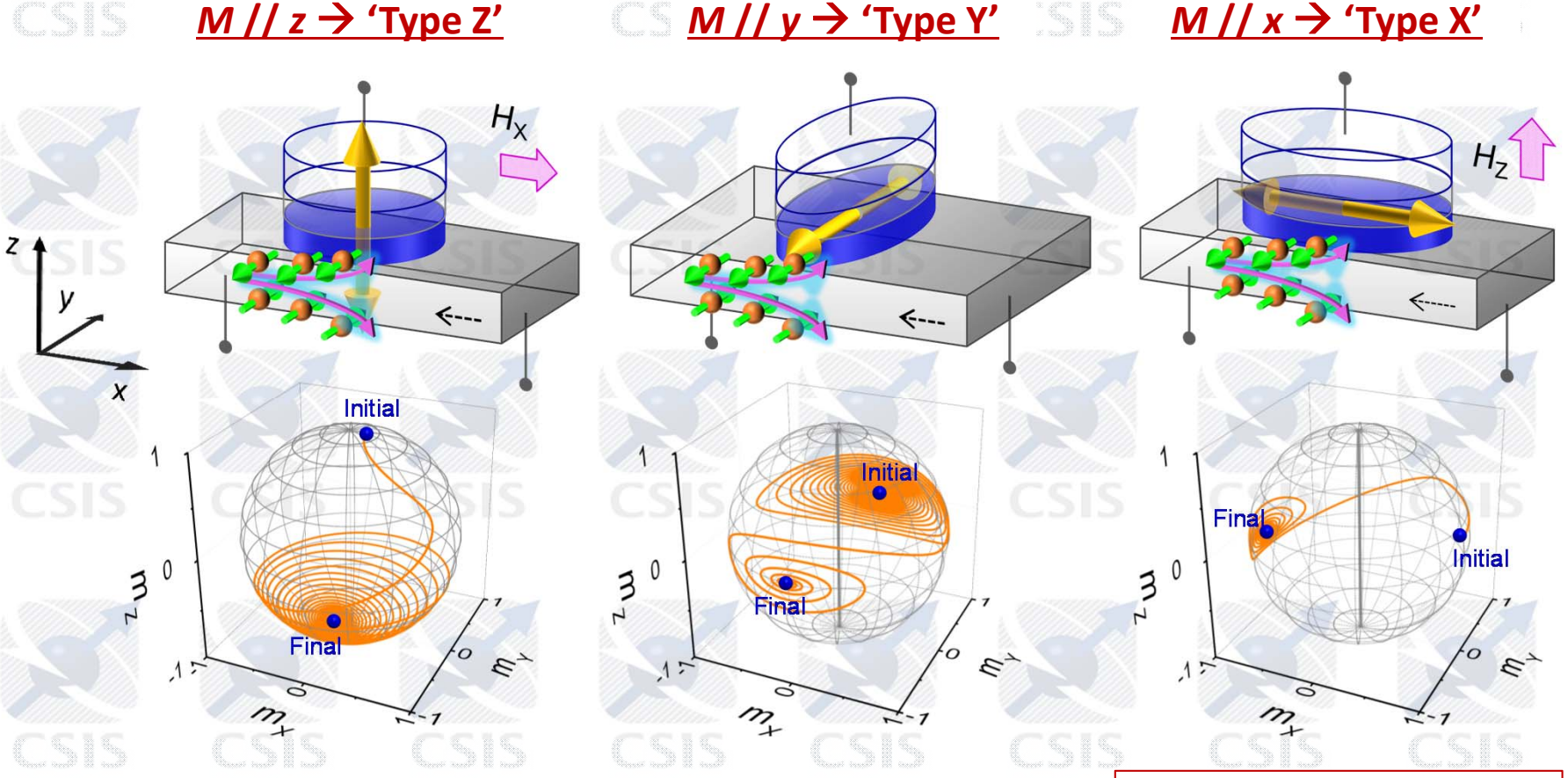
Advantage of 3-terminal device





- TDDB : Time-dependent dielectric breakdown
- EM : Electromigration

The third switching scheme



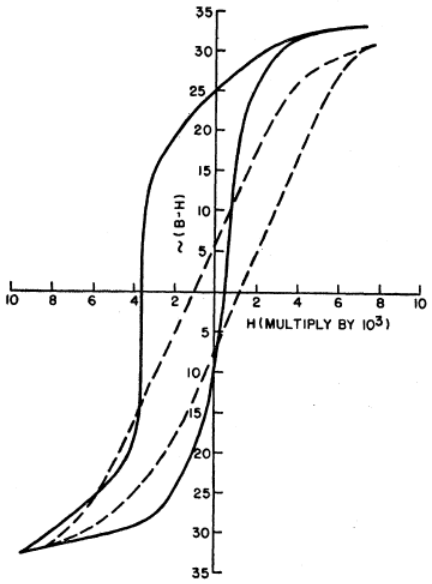
- Type X may serve as
  - tool to explore the physics of SOT switching
  - option for device applications

- ✓ Similar mechanism to Type Z
- ✓ Same material to Type Y

S. Fukami, HO *et al.,* Nature Nanotech. doi: 10.1038/2016.29 (2016).

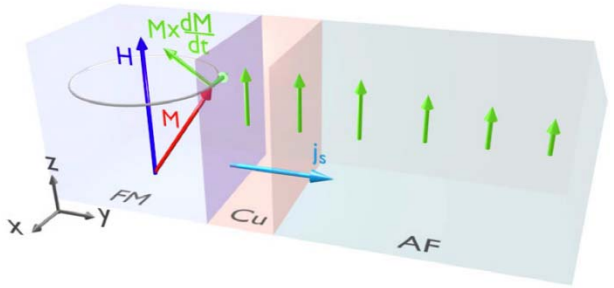
Antiferromagnet (AFM) for SOT switching

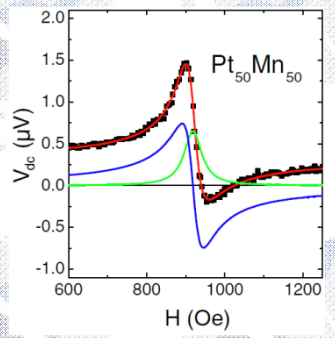
◆ Exchange-bias



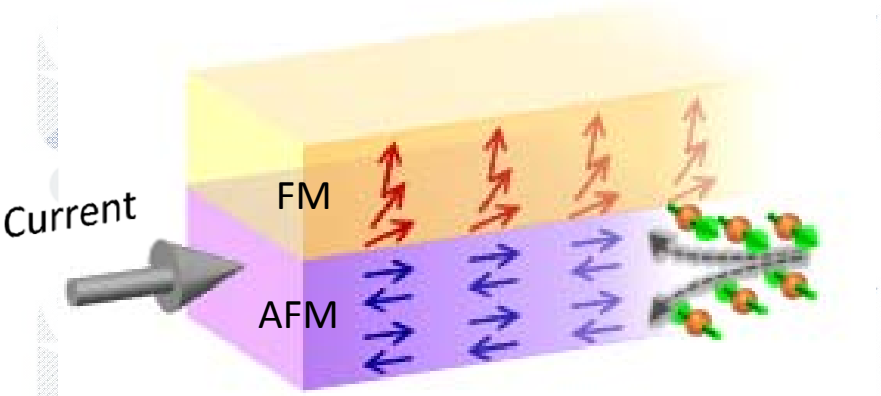
W. H. Meiklejohn et al., Phys. Rev. **102**, 1413 (1956).

◆ Inverse spin Hall effect



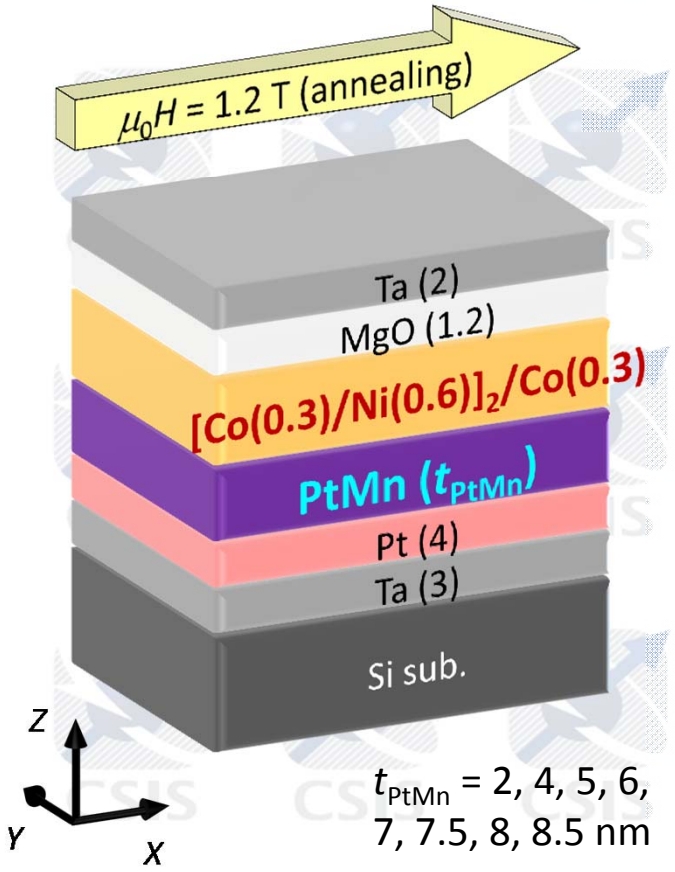


W. Zhang et al., PRL **113**, 196602 (2014).



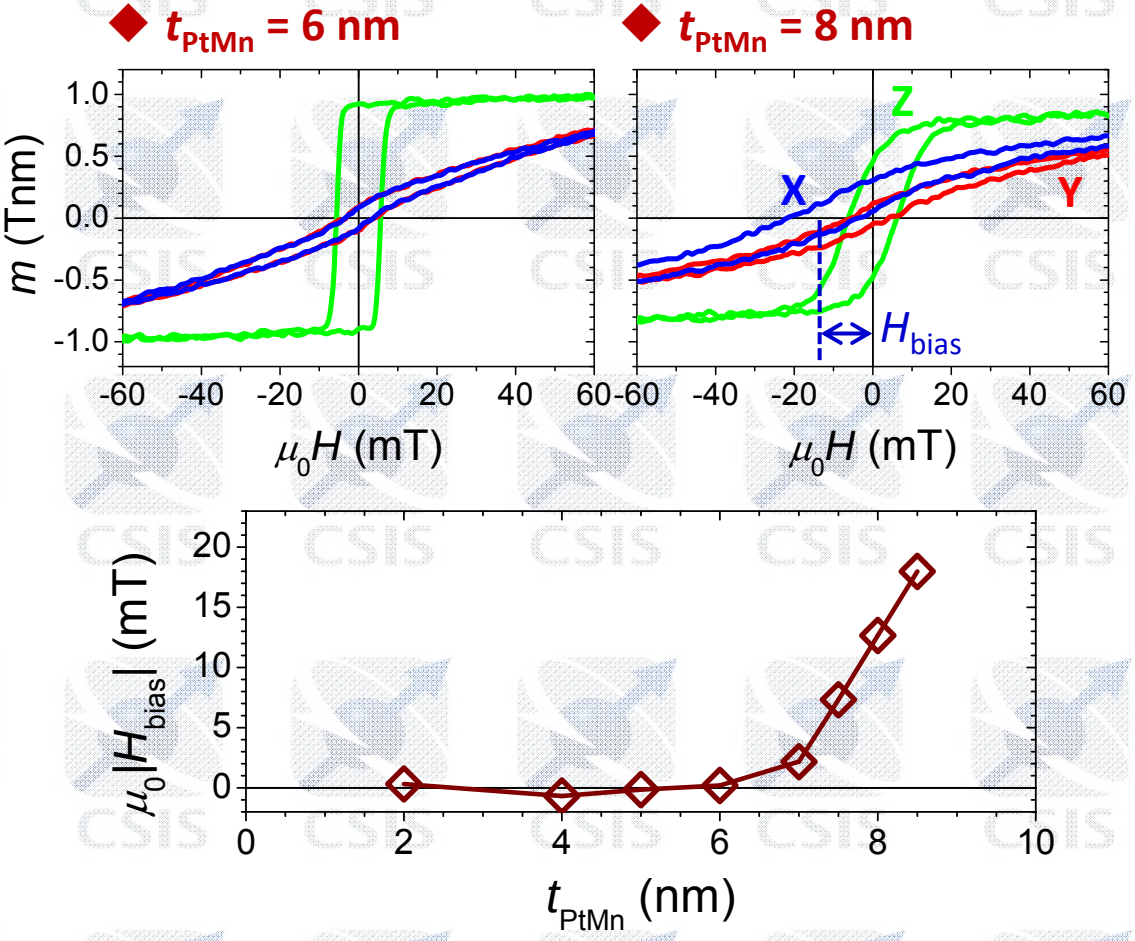
S. Fukami, HO *et al.,* Nature Mater. doi: 10.1038/nmat4566 (2016).

Film stack & *m*-*H* loop



t_{PtMn} = 2, 4, 5, 6, 7, 7.5, 8, 8.5 nm

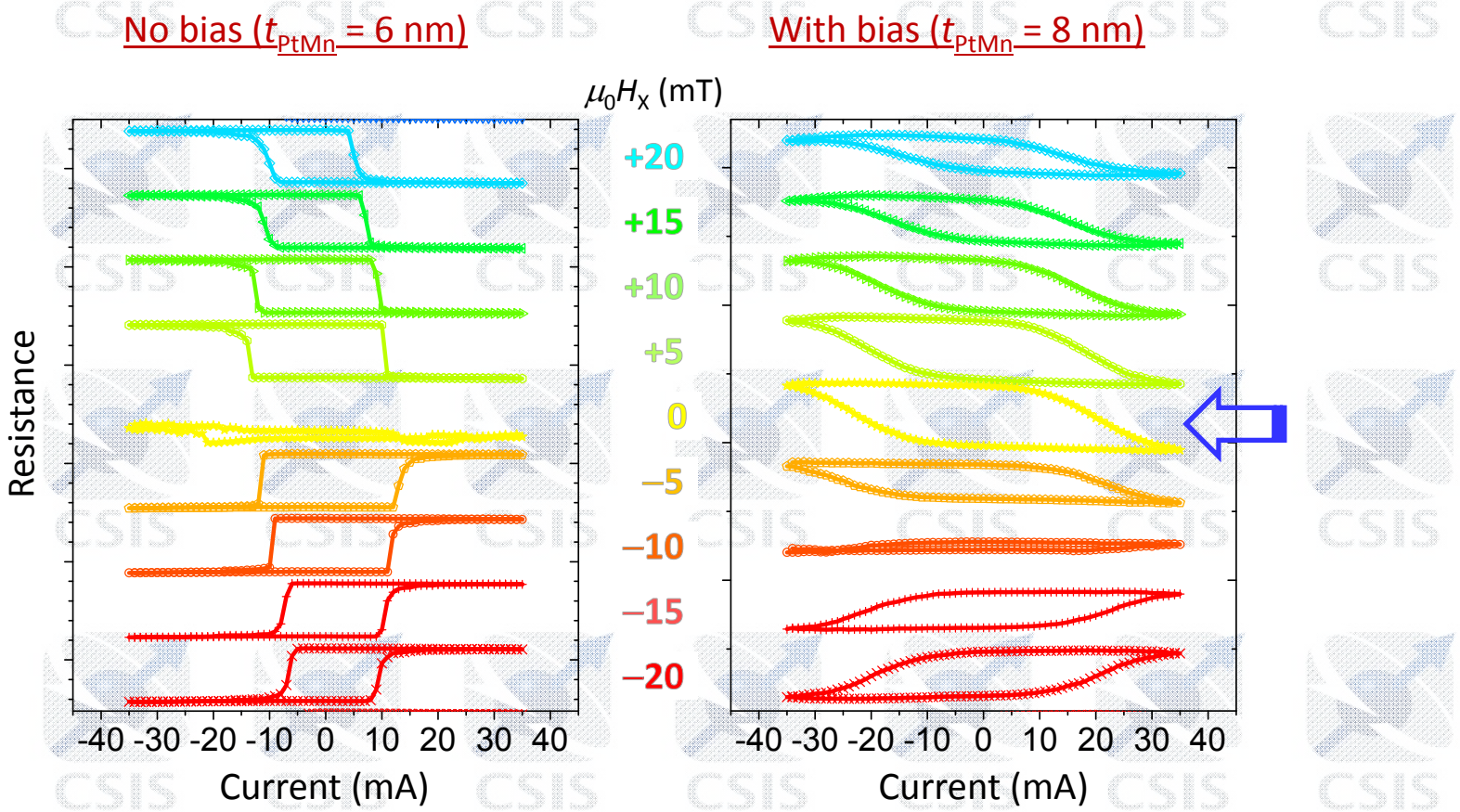
- ✓ dc/rf magnetron sputtering
- ✓ Post annealing (300°C, 2h, 1.2 T)



- ■ Perp easy axis is obtained for all the t_{PtMn}.
- ■ Bias field increases with t_{PtMn} (≥ 7 nm).

S. Fukami, HO *et al.*, Nature Mater. doi: 10.1038/nmat4566 (2016).

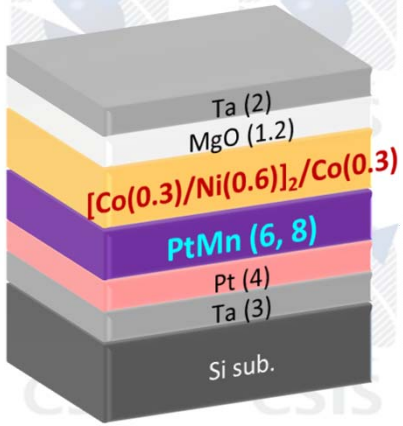
Switching by current under various H_X



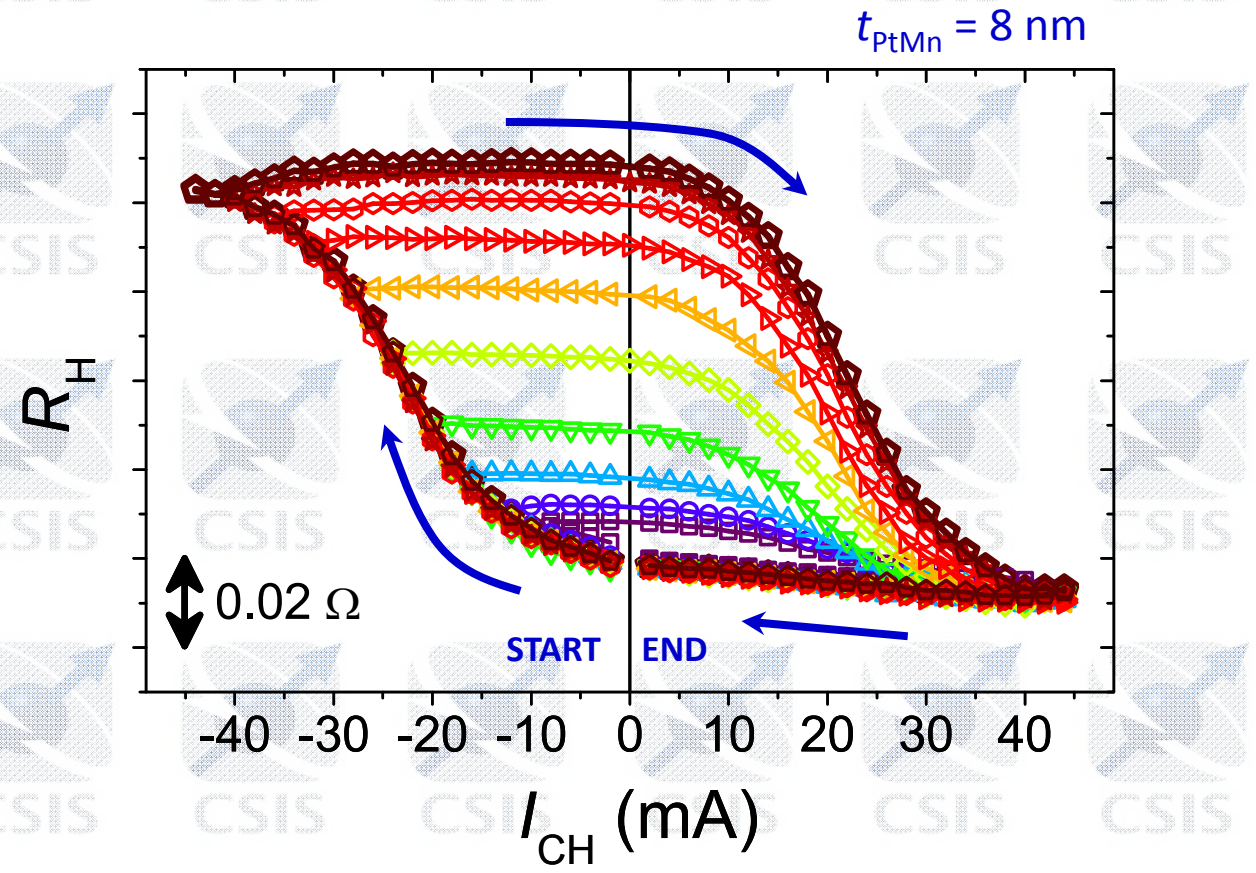
- Field-free switching is observed for exchange-biased device.
- Switching current density is ~10^{10} A/m^2
  … comparable to previous non-magnet/ferromagnet structures

S. Fukami, HO *et al.,* Nature Mater. doi: 10.1038/nmat4566 (2016).

H=0 Switching in Co/Ni-PtMn



- ✓ dc/rf magnetron sputtering
- ✓ Post annealing (300°C, 2h, 1.2 T)

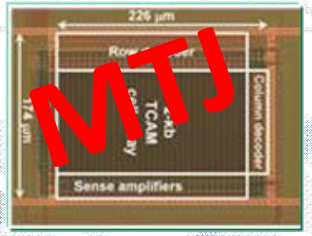


- Spin Hall effect from an antiferromagnet
- Switching without magnetic filed

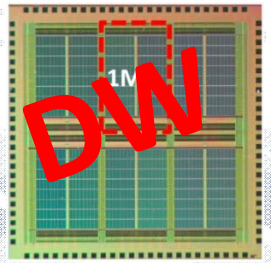
S. Fukami, HO *et al.*, Nature Mater. doi: 10.1038/nmat4566 (2016).

Non-volatile CMOS VLSIs with spintronics

600MHz
MTJ/CMOS Latch
(**Fastest** nonvolatile latch)
(IEDM 2011)

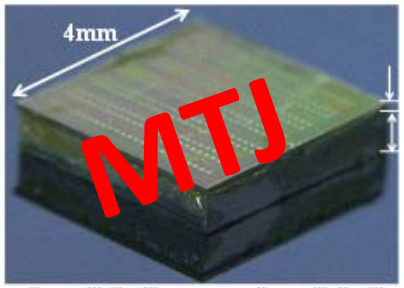


Nonvolatile TCAM
(**Most compact** TCAM cell, 4T-2MTJ)
(VLSI 2011)



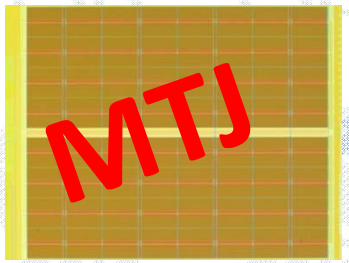
1Mb Array Three Terminal **DW** Cell
(**High endurance**)
(VLSI 2012)

First Auto **Design Tool** for Spintronics CMOS
(2011)

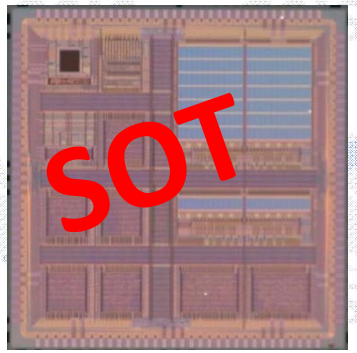


Nonvolatile FPGA
with TSV
(**First 3D** Spintronics CMOS Processor)
(VLSI 2012)

Nonvolatile GPU
(**Largest Scale** Spintronics Random Logic 500kgate/chip)
(ISSCC 2013)



1.5nsec / 1Mbit
Embedded MRAM
(**Fastest** nonvolatile 1Mbit memory)
(VLSI 2013)



Nonvolatile microcomputer
(**First** nonvolatile microcomputer)
(ISSCC 2014)

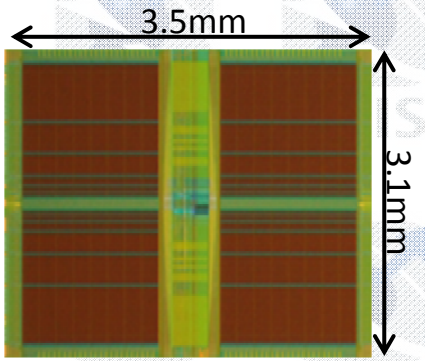
Delay × Power × Area Ratios

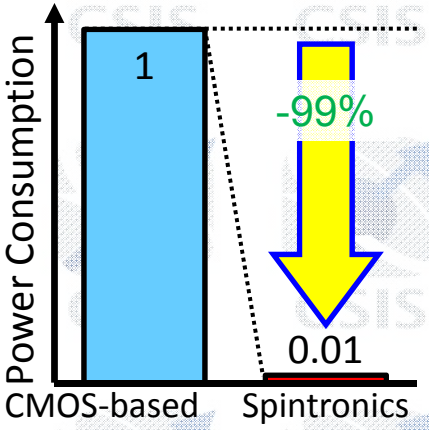
TOHOKU UNIVERSITY

NV-TCAM

2013 Symposium. on VLSI Circuits

Non-volatile VLSIs for search engine for big data





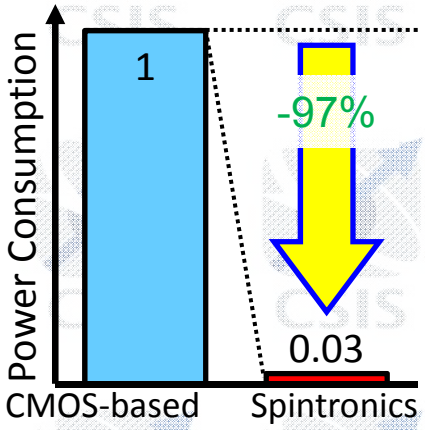
$1 \times \frac{1}{100} \times 1 \leqq \frac{1}{64}$
(delay) (power) (area)

※in case of used for full text search system

NV-FPGA

2013 IEICE Electronics Express

Non-volatile field programmable gate array (FPGA)



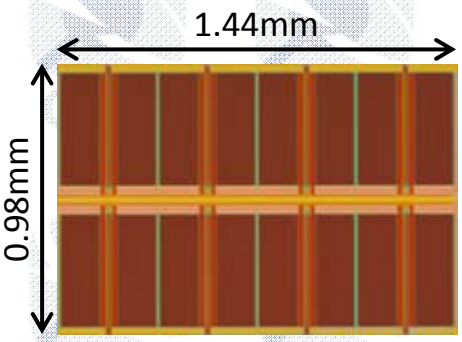
$1 \times \frac{1}{32} \times \frac{1}{2} \leqq \frac{1}{64}$
(delay) (power) (area)

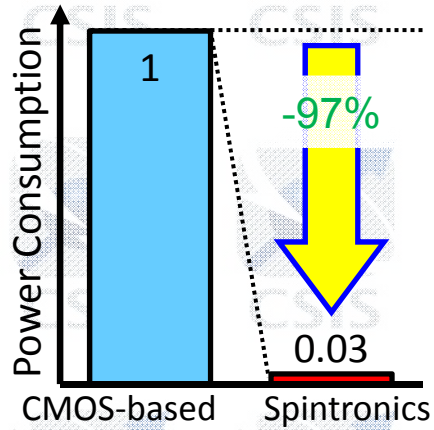
※ in case of implementation to a typical application

STT-MRAM

2012 Symposium. on VLSI Circuits

Non-volatile cash memory embedded in high speed CPU





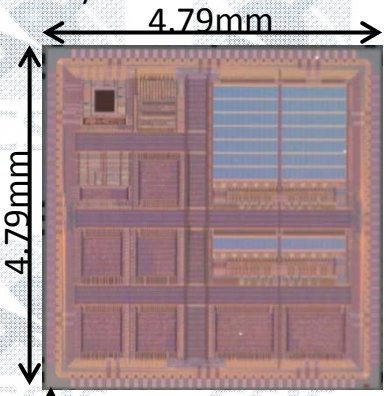
$\frac{1}{1.5} \times \frac{1}{29} \times \frac{1}{1.7} \leqq \frac{1}{64}$
(delay) (power) (area)

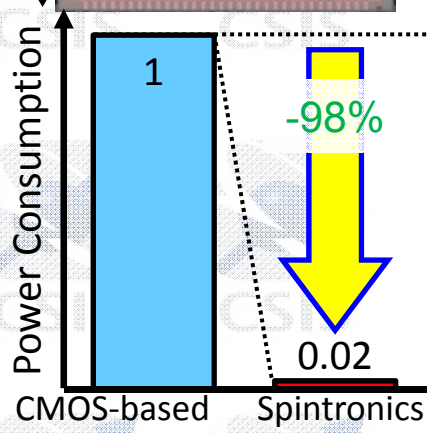
※in case of typical cash operation

NV-MPU

2014 IEEE ISSCC

Non-volatile microcontroller for battery-driven sensor device

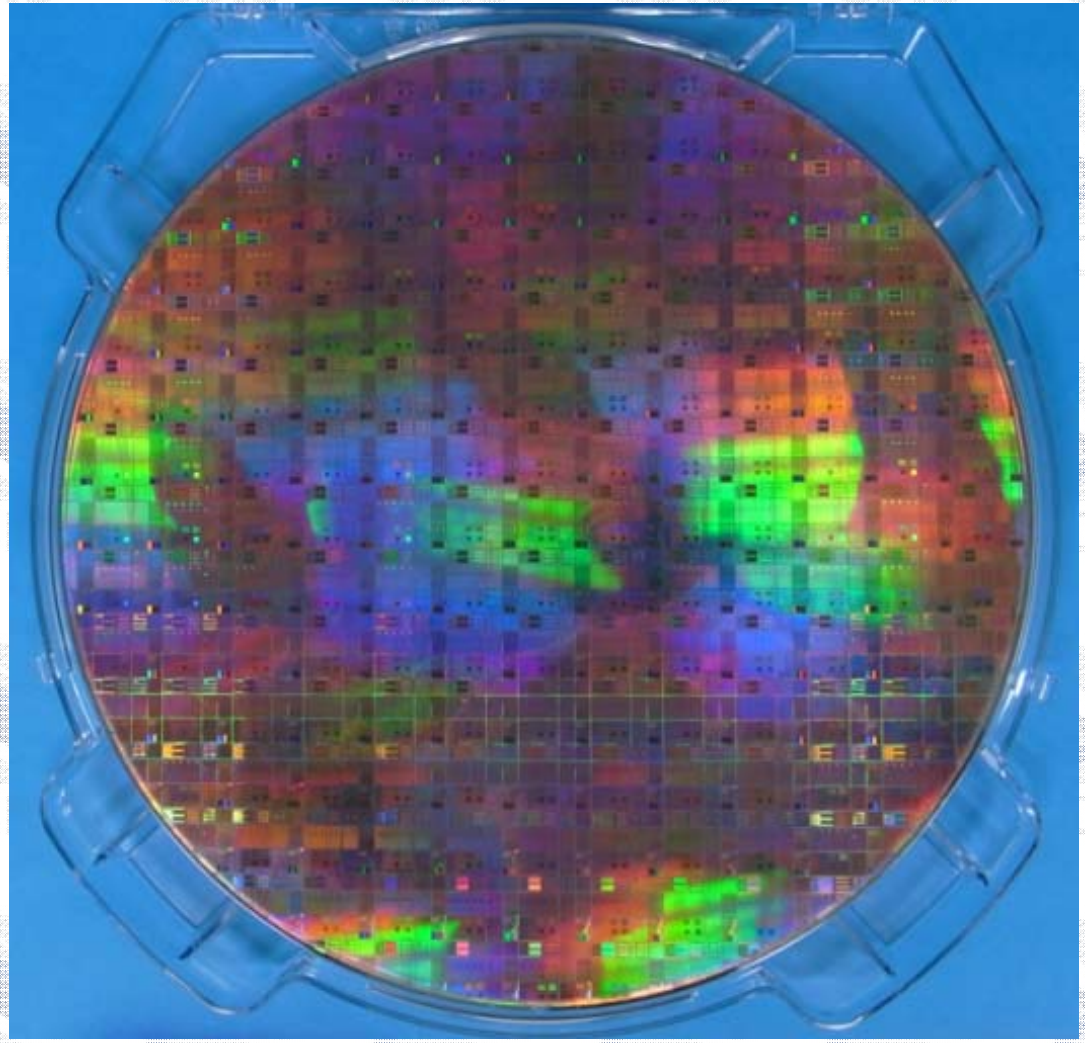




$1 \times \frac{1}{80} \times 1 \leqq \frac{1}{64}$
(delay) (power) (area)

※in case of use in a wireless sensor device

On 300 mm wafers



Paradigm Shift of VLSI by Spintronics