MTJ-Based Nonvolatile Logic-in-Memory Architecture

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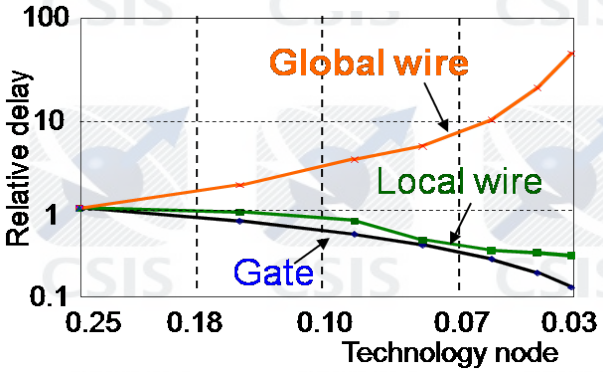
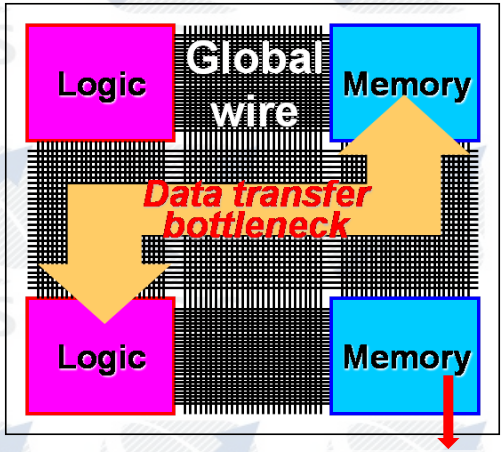
Outline

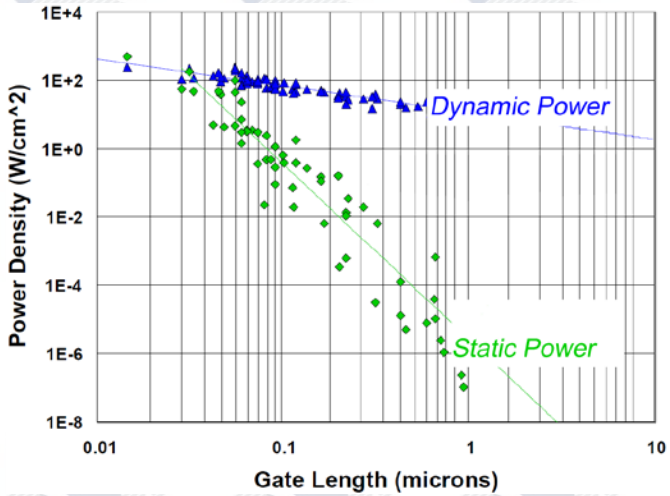
- **Nonvolatile Logic-in-Memory Architecture Overview**
- NV GP-Logic: Nonvolatile-FPGA
- NV SP-Logic: Nonvolatile-TCAM
- Conclusions & Future Prospects

Background: Increasing delay & power





Leakage current



Logic and **Memory** modules are separated
Many **interconnections** between modules

Wire delay dominates chip performance
Global wires requires **large drivers**.

Delay: **Long** Power: **Large**

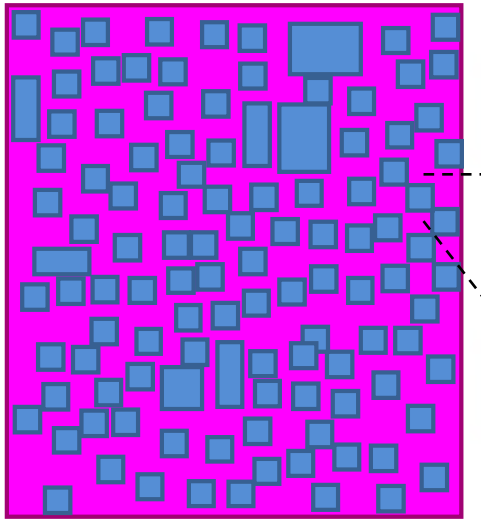
On-chip memory modules are **volatile**.

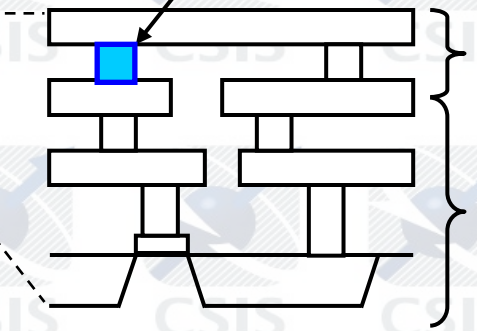
Power supply must be **continuously** applied in memory modules.

Static power: Large

Nonvolatile logic-in-memory architecture

- **Logic-in-Memory Architecture (proposed in 1969):**
  Storage elements are distributed over a logic-circuit plane.

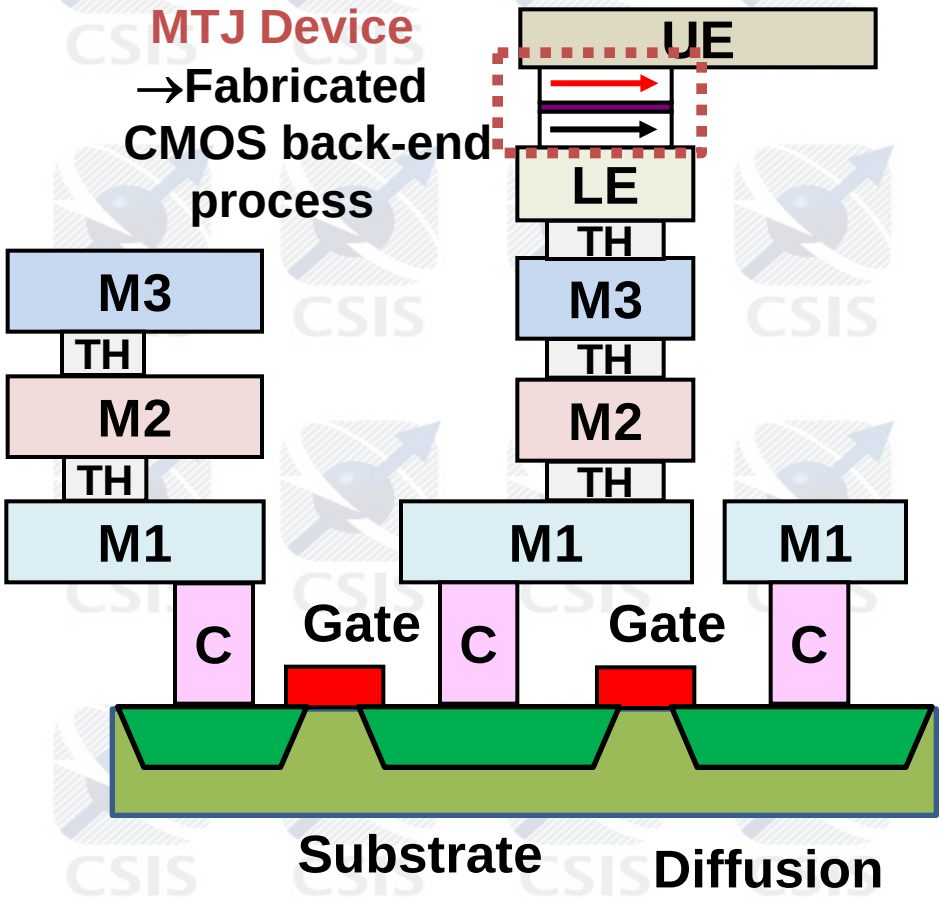




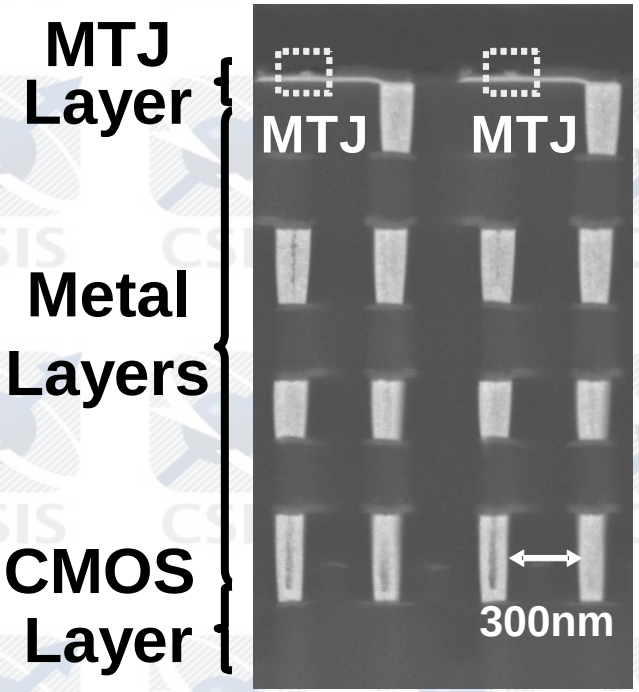
- **No volatility**
- **Unlimited endurance**
- **Fast writability**
- **Scalability**
- **CMOS compatibility**
- **3-D stack capability**

- Storage is nonvolatile:
  (Leakage current is cut off) → Static power is cut off.
- MTJ devices are put on the **CMOS** layer → Chip area is reduced.
- Storage/logic are merged:
  (global-wire count is reduced) → Wire delay is reduced.
  → Dynamic power is reduced.

Implementation of MTJ Device



MTJ device stacked over MOS Plane

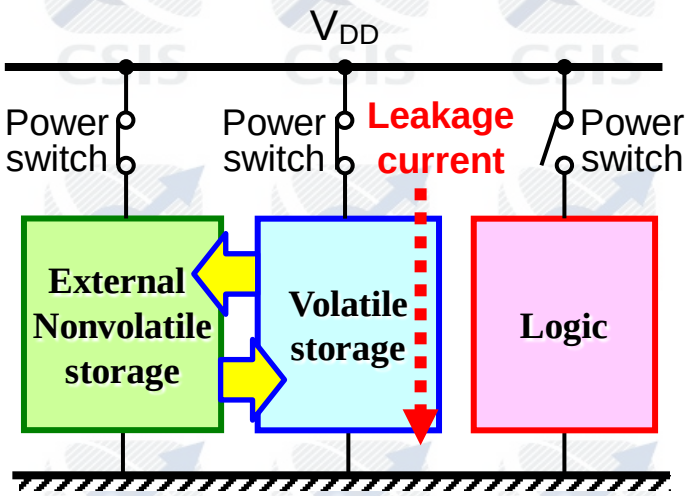


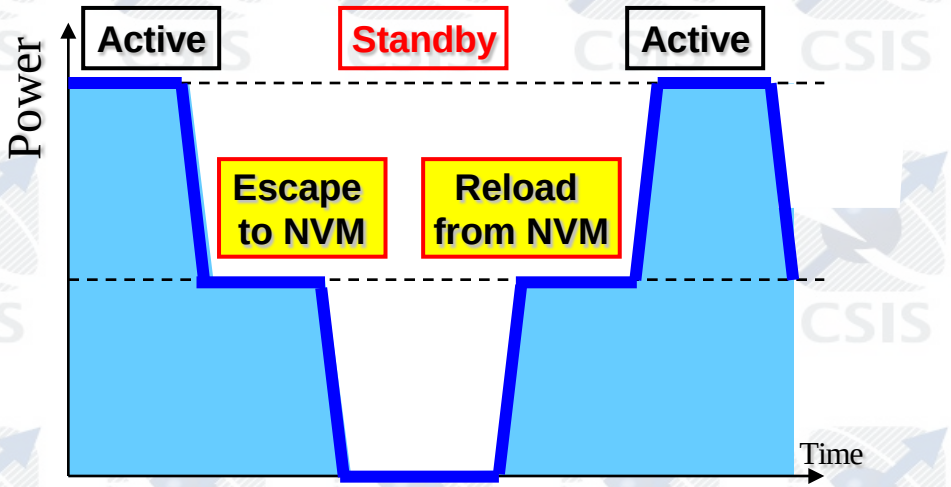
D. Suzuki, et al., VLSI Circuit Symp. 2009

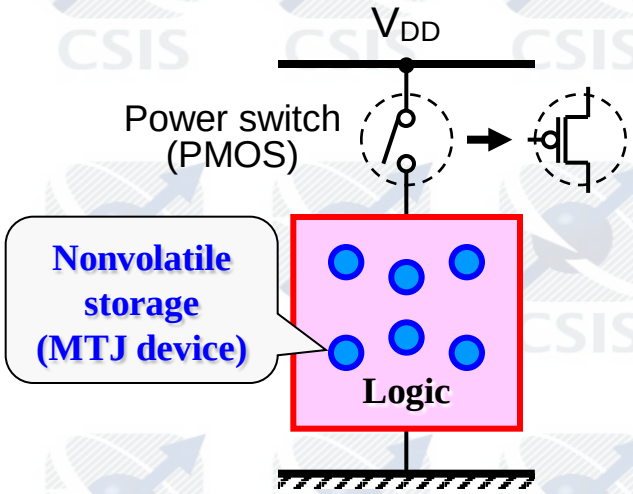
Cross-sectional SEM image

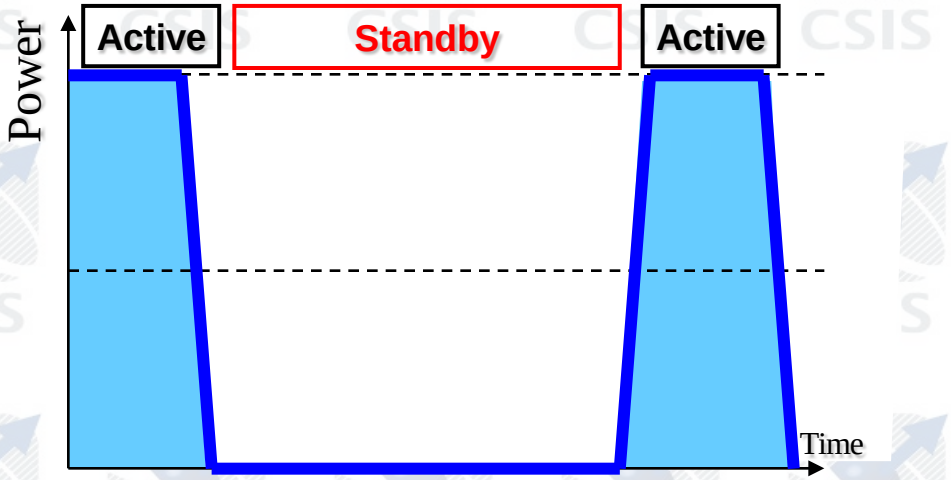
The area cost using MTJ device is small.

Power-Gating Suitability





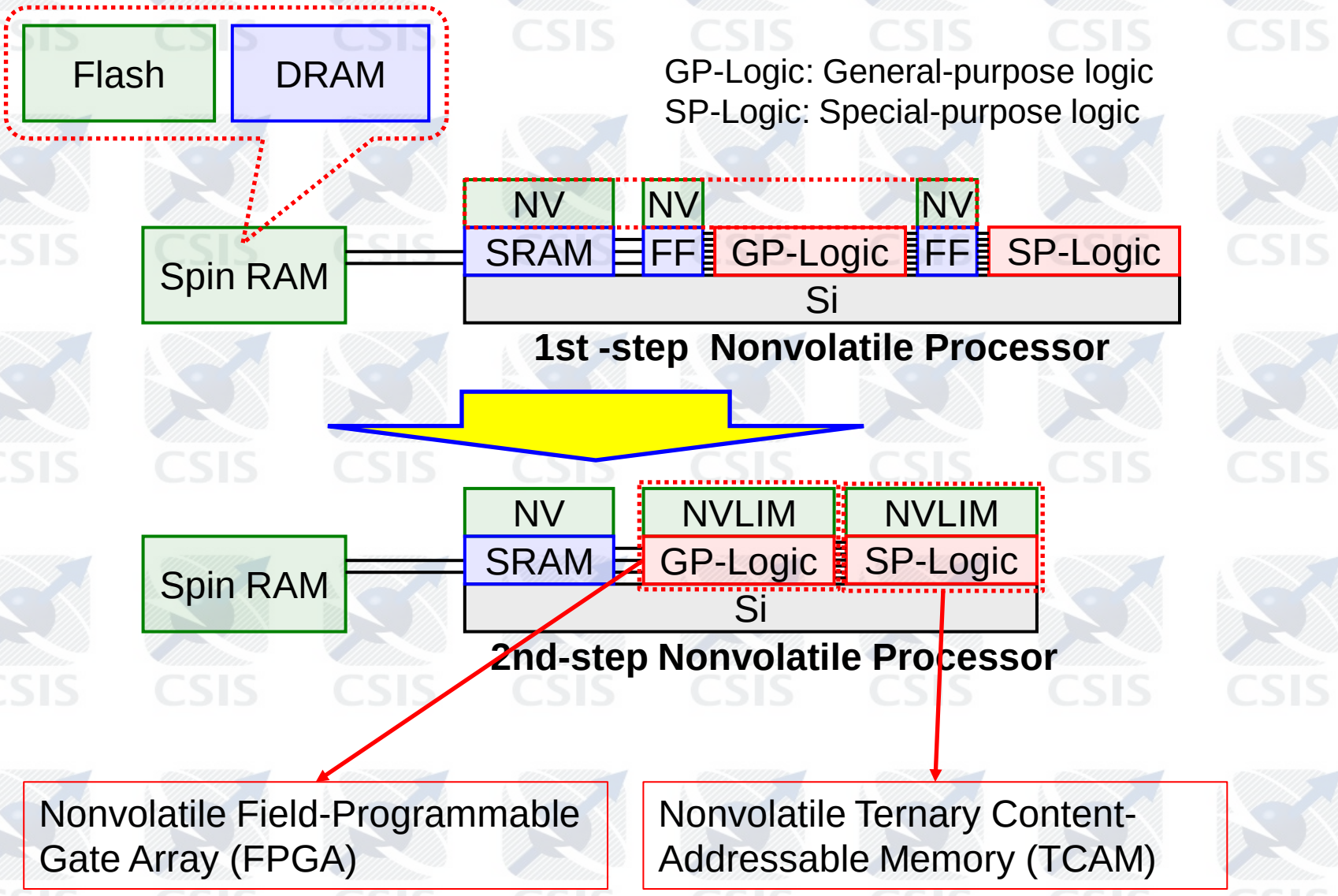




NV logic-in-memory architecture

⇨ Power gating is performed without data backup/reload.

Nonvolatile Processor Architecture



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- Nonvolatile Logic-in-Memory Architecture Overview
- **NV GP-Logic: Nonvolatile-FPGA**
- NV SP-Logic: Nonvolatile-TCAM
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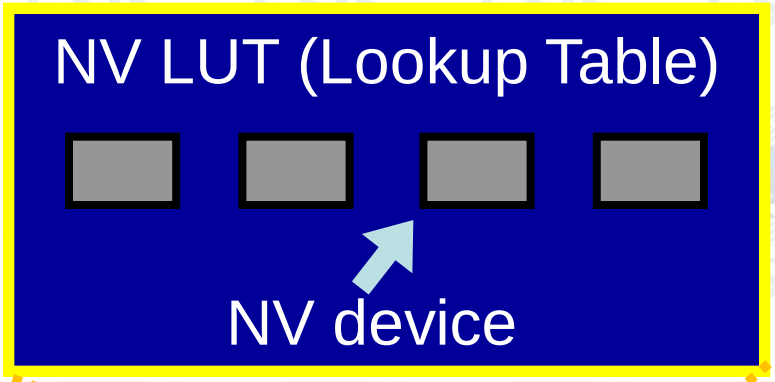
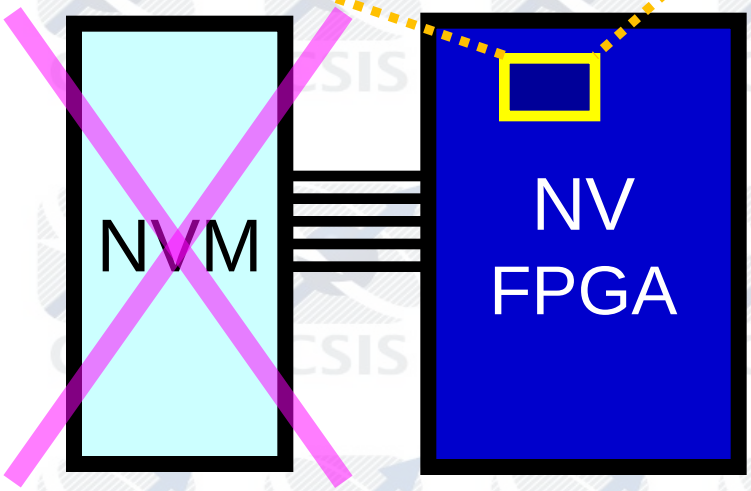
Nonvolatile Field-Programmable Gate Array (FPGA)



-- Arbitrary logic functions are performed and programmed by FPGA
-- Power dissipation and hardware overhead are two major issues.
-- NV storage elements are distributed over the NV-FPGA (no external NVM).



Not required!

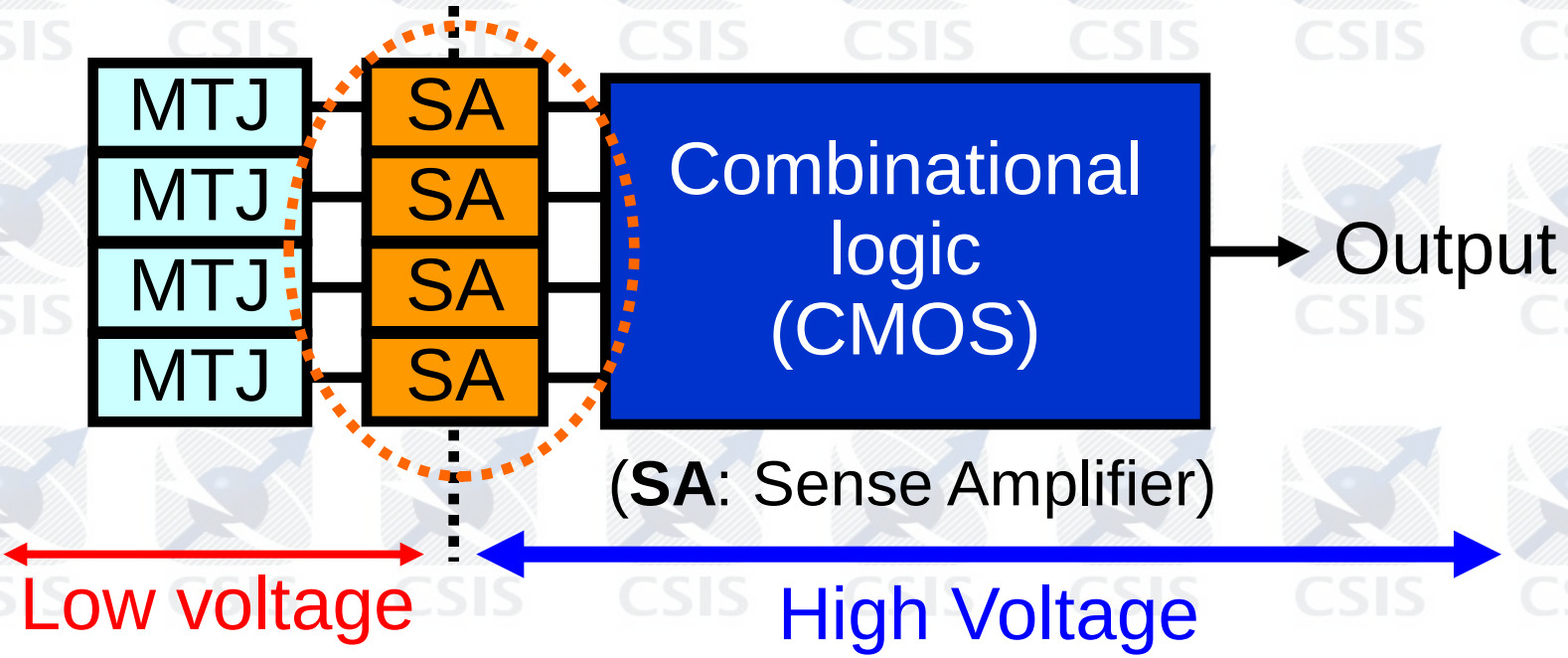
☺ **Leakage** current **elimination** and **short latency** are possible.

☹ How to design?

Nonvolatile logic-in-memory architecture

Conventional nonvolatile FPGA

☹ CMOS logic circuit requires **high-voltage** input swing.

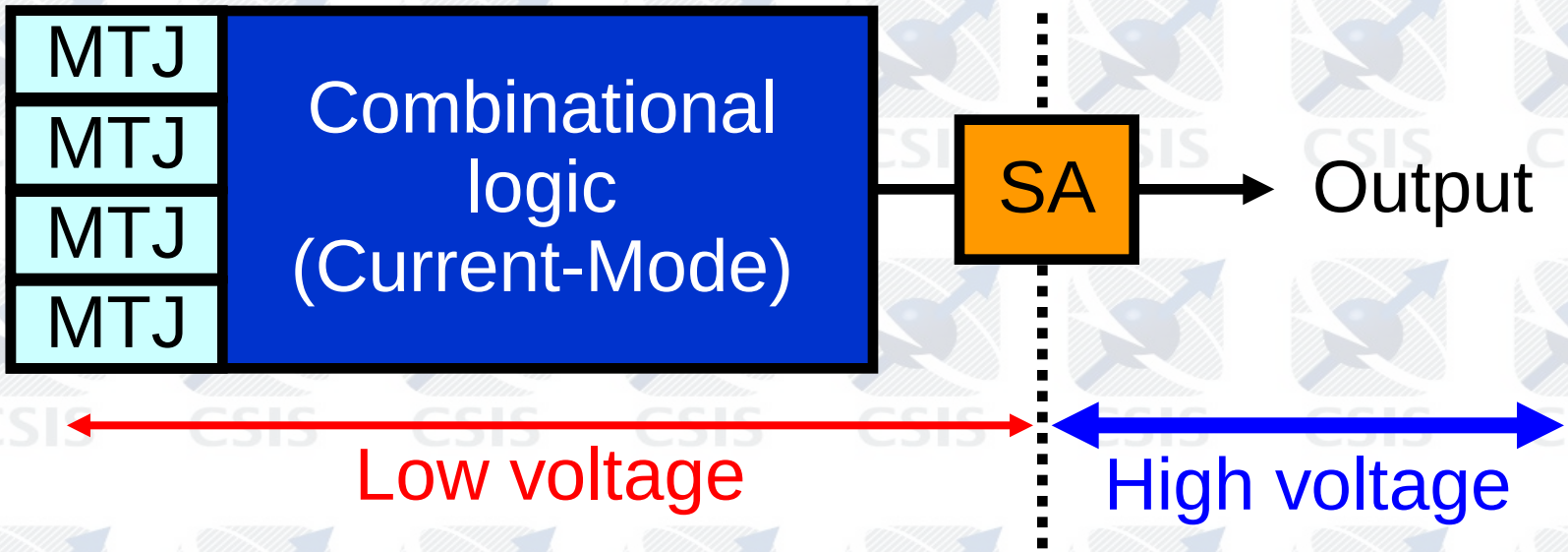


How do we perform logic operation by using low swing signal from MTJ device directly?

MOS/MTJ-hybrid circuitry (Proposed)

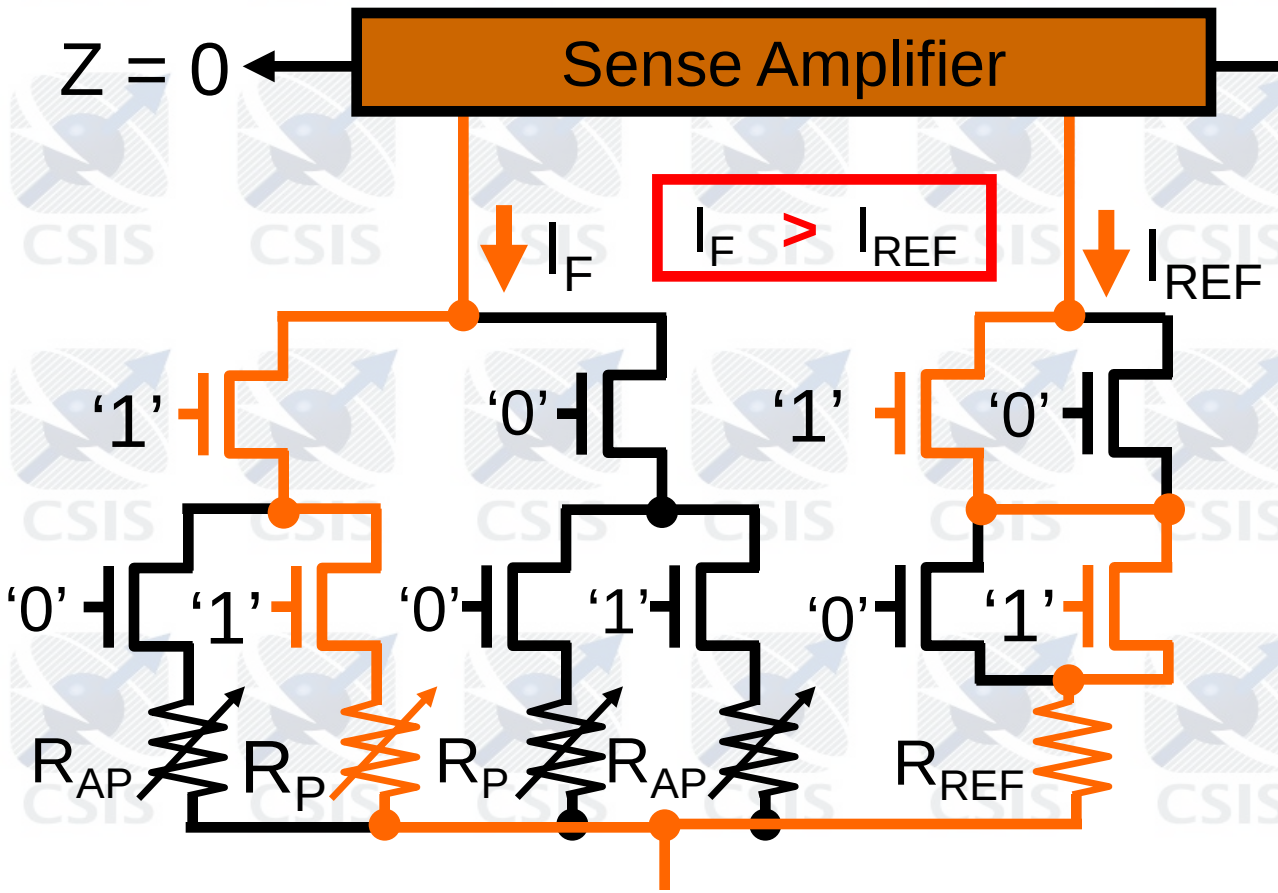
Current-mode logic (CML)

☺ Logic operation is performed even low swing voltage by using the small difference of the current value.



Device count is reduced to 28% with less performance degradation.

Operation example (XOR)



Truth table

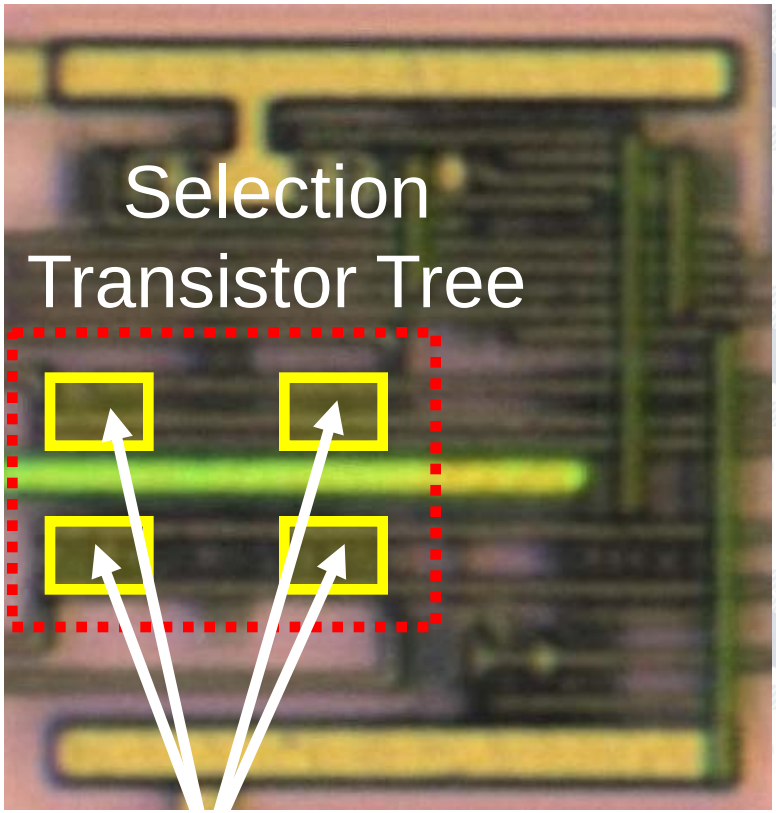
A	B	Z
0	0	1
0	1	0
1	0	0
1	1	1

Logic operation in low swing voltage is performed by using a MOS/MTJ-hybrid network.

Test chip features

D. Suzuki, et al., VLSI Circuit Symposium, June 2009.

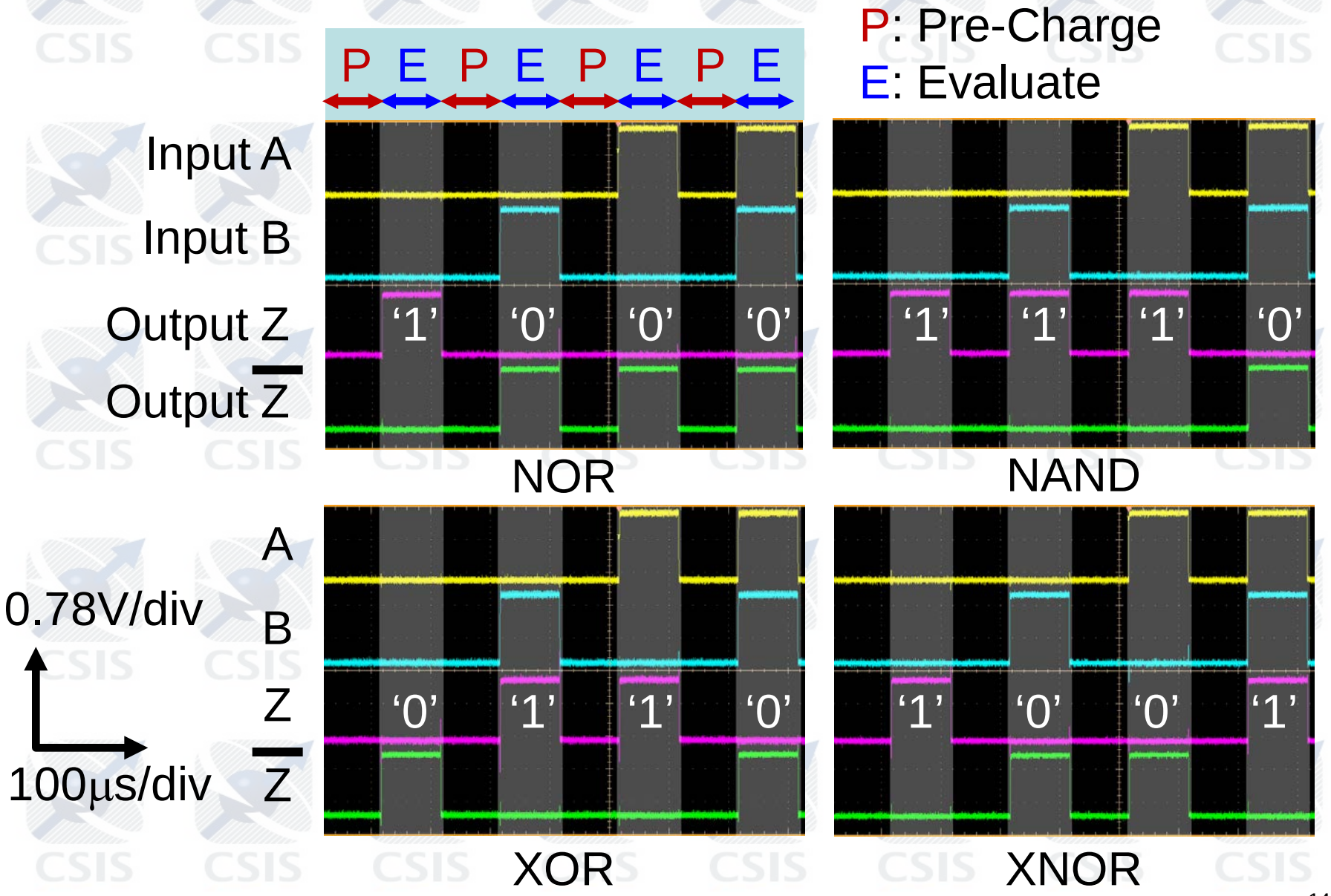
Fabricated 2-input LUT



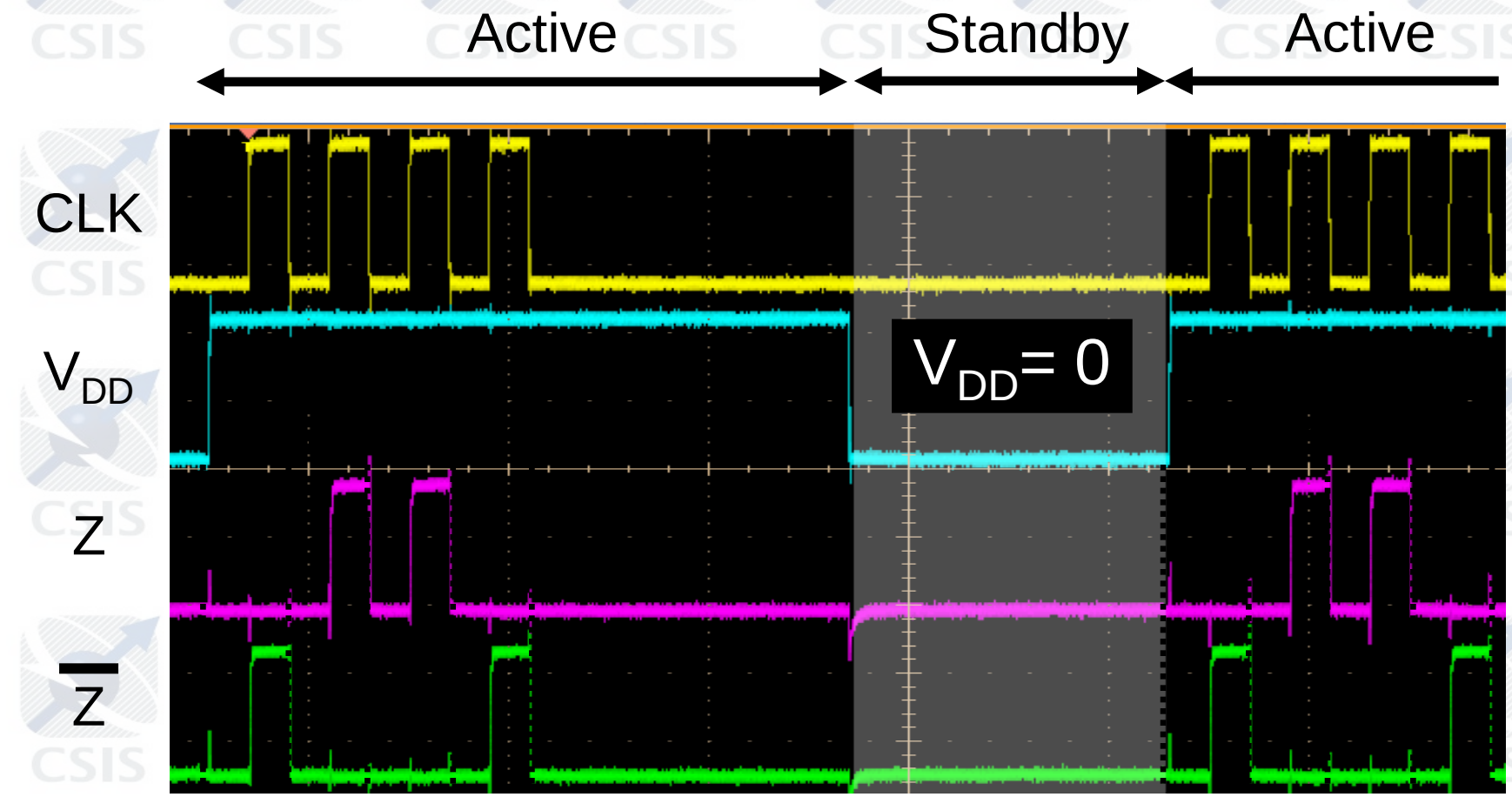
4 MTJ devices are stacked over MOS layer

Process		0.14μm MTJ/MOS 1-Poly, 3-Metal
Area		287μm²
MTJ Size		50nm ×150nm
TMR Ratio		100%
Write	Current	150μA
	Time	10ns
Standby Current		0A

Measured waveforms (Basic operations)



Immediate wakeup behavior



Immediate wakeup behavior has also measured successfully.

Comparison of performances

		Nonvolatile SRAM *1)	Proposed
Device Counts		102 MOSs + 8 MTJs	29 MOSs + 4 MTJs
Area *2)		702 μm^2	287μm^2
Active	Delay *3)	140 ps	185 ps
	Power*3)	26.7 μW	17.5 μW
Standby	Power	0 μW	0 μW

*1) W. Zhao, et al., Physica Status SOLIDI a Application and Materials Science, 205, 6, 1373/1377, May 2008.
*2) Estimation based on a 0.14μm process
*3) HSPICE simulation based on a 0.14μm MOS/MTJ-hybrid process

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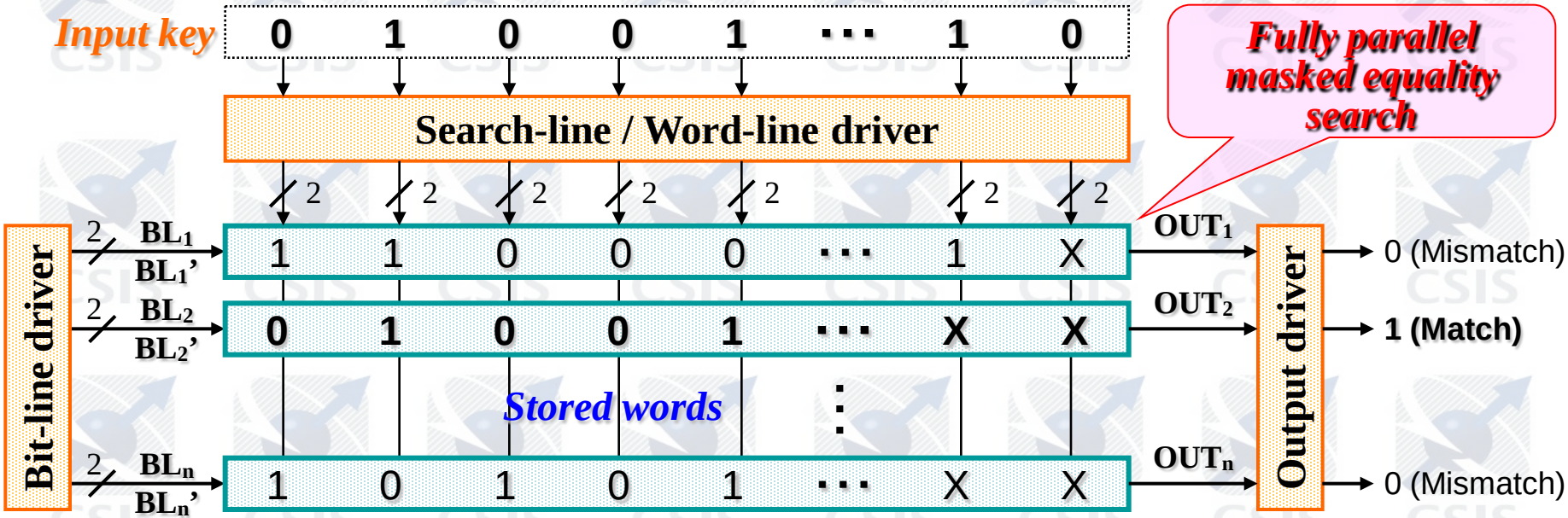
Ternary Content-Addressable Memory (TCAM)



Fully parallel search and fully parallel comparison can be done.

TCAM is a "functional memory."

TCAM is the powerful data-search engine

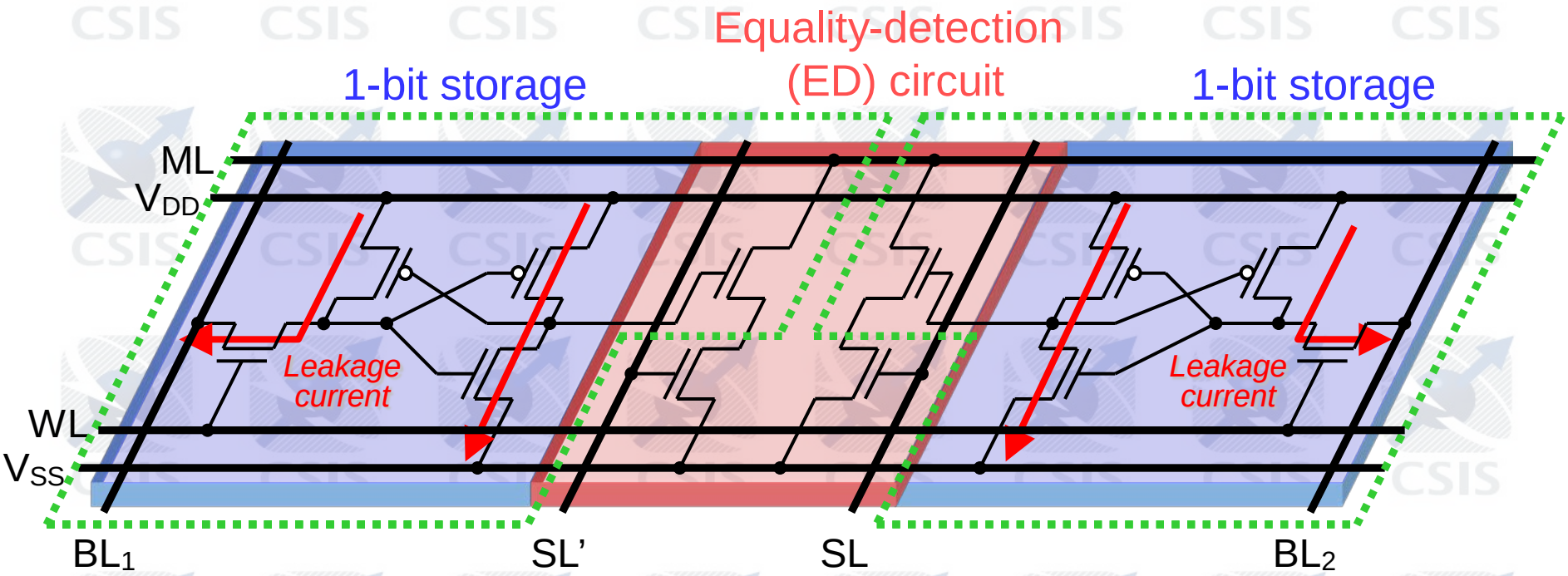
⇨ useful for various applications such as database machine and virus checker in network router

TCAM must be implemented more **compactly** with **lower power** dissipation.

NV-TCAM Cell Function

Stored data		Search input	Current comparison	Match result
B	**(b_1,b_2)**	**S**		**ML**
0	**(0,1)**	**0**	$I_Z < I_Z'$	**1** *(Match)*
		1	$I_Z > I_Z'$	**0** *(Mismatch)*
1	**(1,0)**	**0**	$I_Z > I_Z'$	**0** *(Mismatch)*
		1	$I_Z < I_Z'$	**1** *(Match)*
X (**don't care**)	**(0,0)**	**0**	$I_Z < I_Z'$	**1** *(Match)*
		1	$I_Z < I_Z'$	**1** *(Match)*

CMOS-based TCAM cell circuit

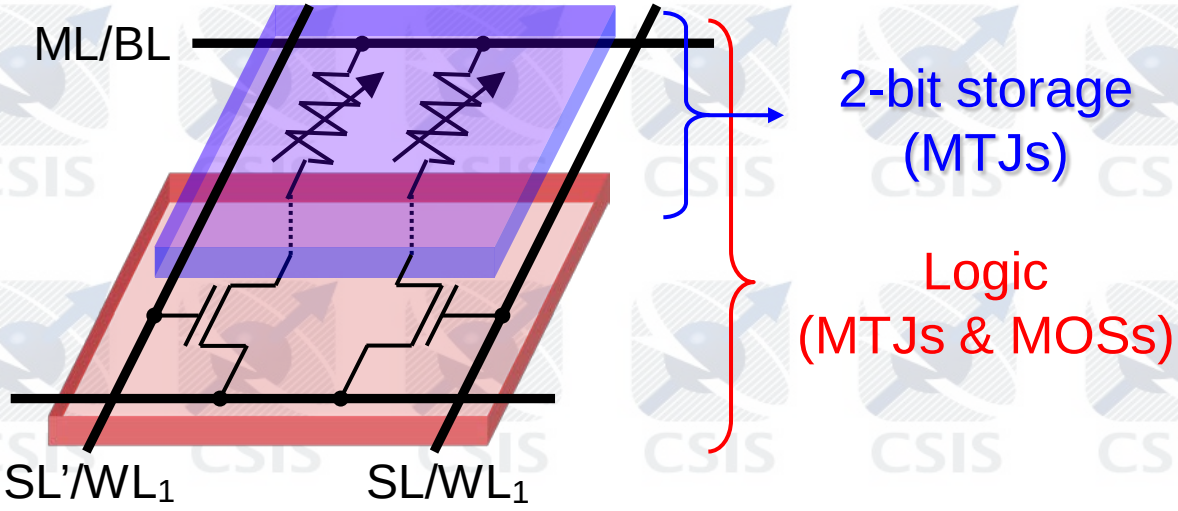


- Transistor counts : **12** (ED;4T, 2-bit storage;8T)
- Input/output wires : **8** (BL;2, WL;1, V_{DD}&V_{SS};2, SL;2, ML;1)
- Always supply the power : **Many leakage current path**

How to realize compact & cut off the leakage current ?

MOS/MTJ-hybrid TCAM cell circuit

S. Matsunaga, et al. Applied Physics Express (APEX), 2, 2, 023004, Feb. 2009.

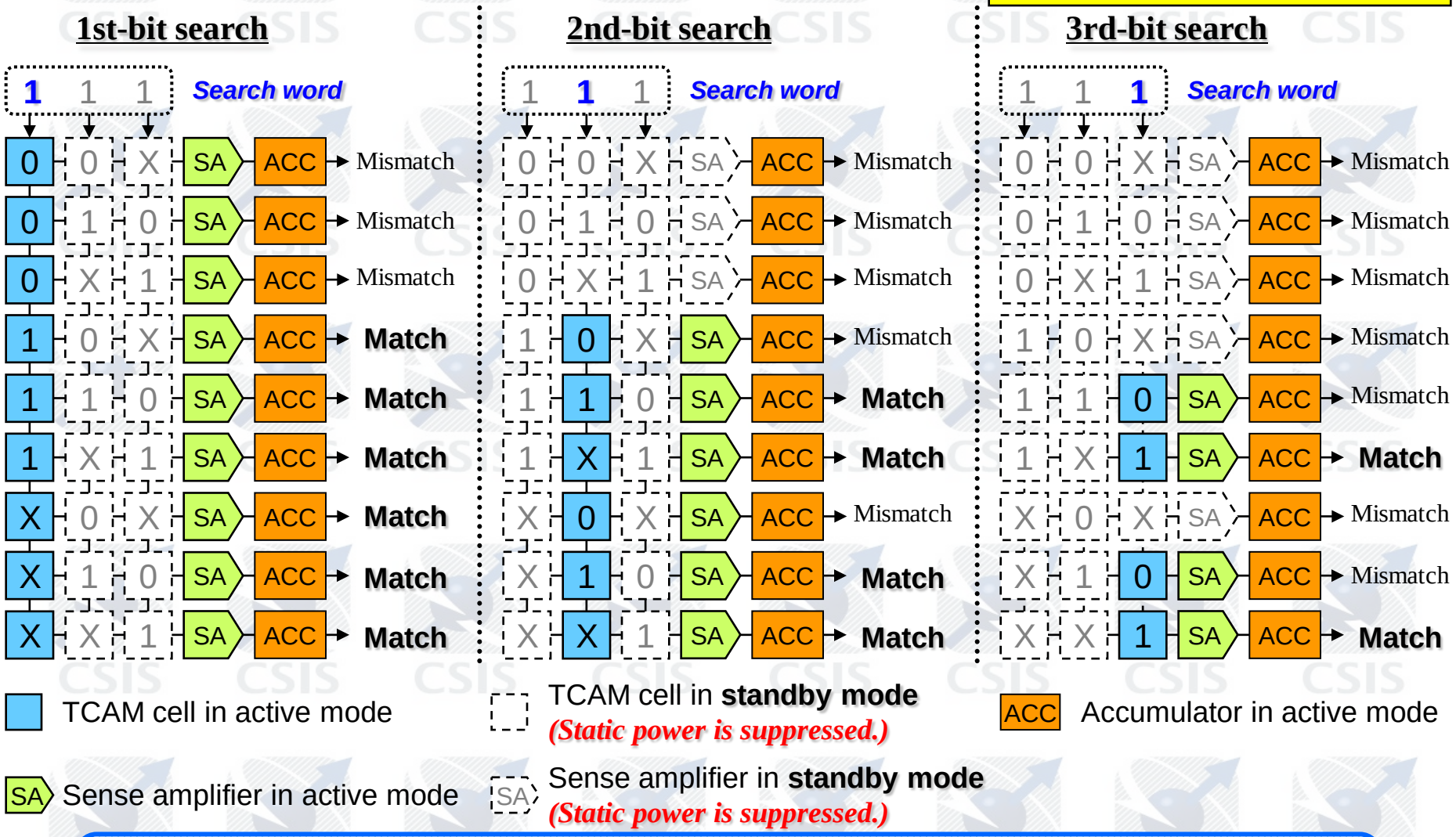


- **Merge storage into logic circuit : Compact (2T-2MTJ)**
- **Share wires : 4 (ML/BL, SL/WL, No-V_{DD})**
- **3-D stack structure : Great reduction of circuit area**

Compact & nonvolatile TCAM cell with MTJ devices

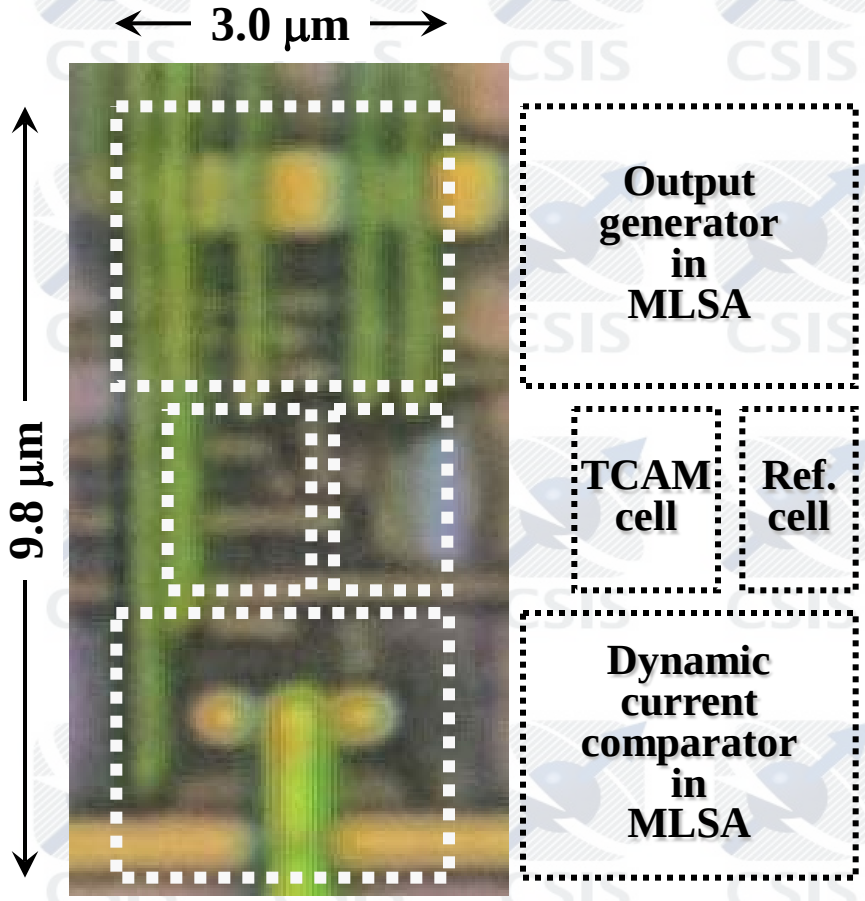
Power-Gating Scheme of Bit-Serial NV-TCAM

S. Matsunaga, et al., JJAP 49 (2010) 04DM05.



According to the word length of the TCAM,
the effectiveness of the standby-power reduction is increased.

TCAM cell circuit test chip



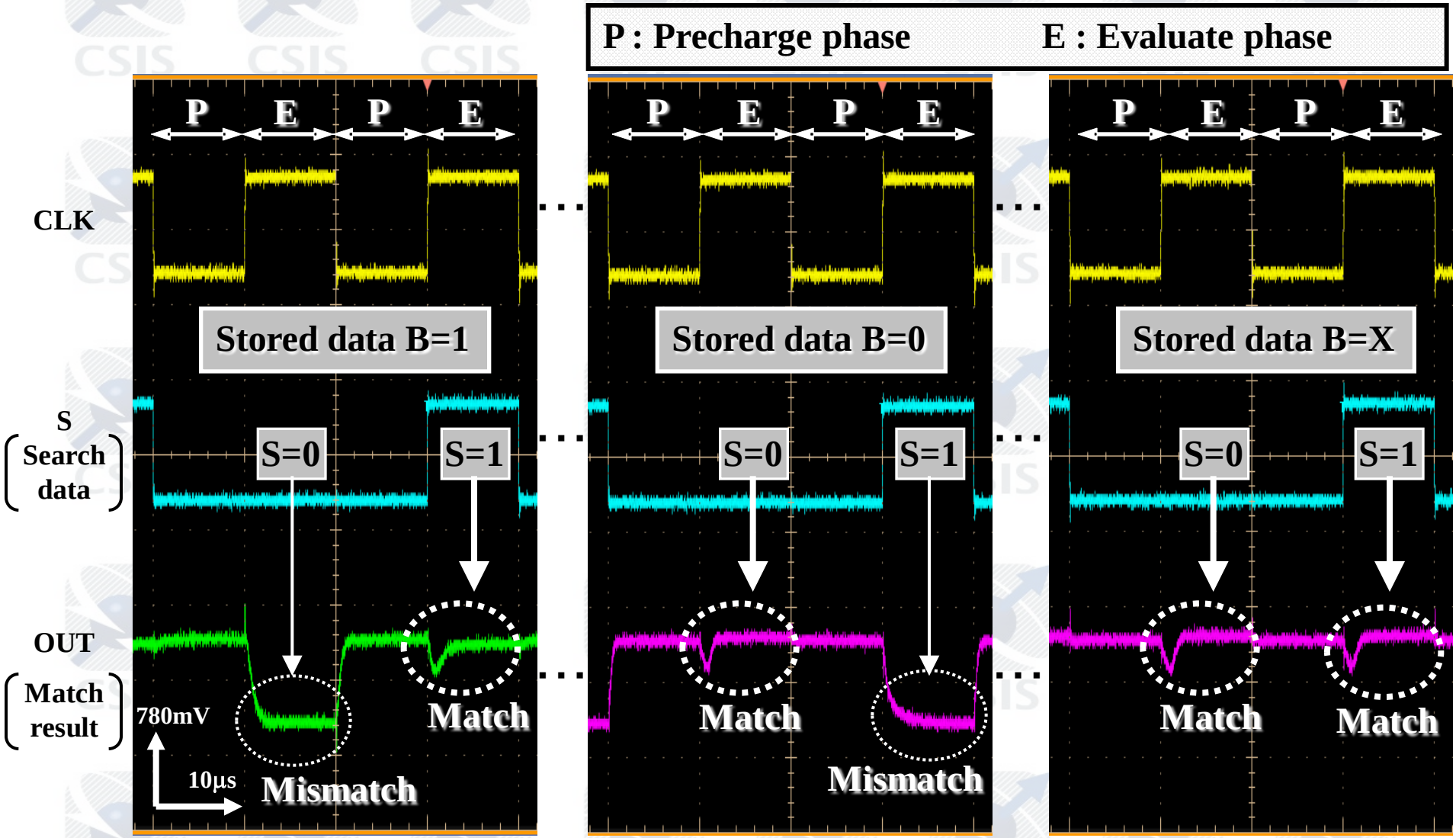
Chip features

Process	0.14μm CMOS/MTJ 1-Poly, 3-Metal
Total area	29.4 μm^2
TCAM cell size	3.15 μm^2 (2.1 μm × 1.5 μm) [a)]
Cell structure	2MOSs-2MTJs
MTJ size	50 nm × 200 nm
TMR ratio	167 %
Average write current	274 μA (τ_p = 10 μs) [b)]
Standby current	0A (Power off)

[a)] A CMOS-based TCAM cell with 12 transistors, whose cell size is 17.54 μm^2 under a 0.18 μm CMOS process, has been reported.[8)] The size of the conventional TCAM cell can be estimated as 10.61 μm^2 under a 0.14 μm CMOS process by scaling down. Thus, the size of the fabricated TCAM cell is reduced to 30 % compared to that of the conventional one. Moreover, minimum size of the proposed TCAM cell can be considered as 1/6 of the conventional one.

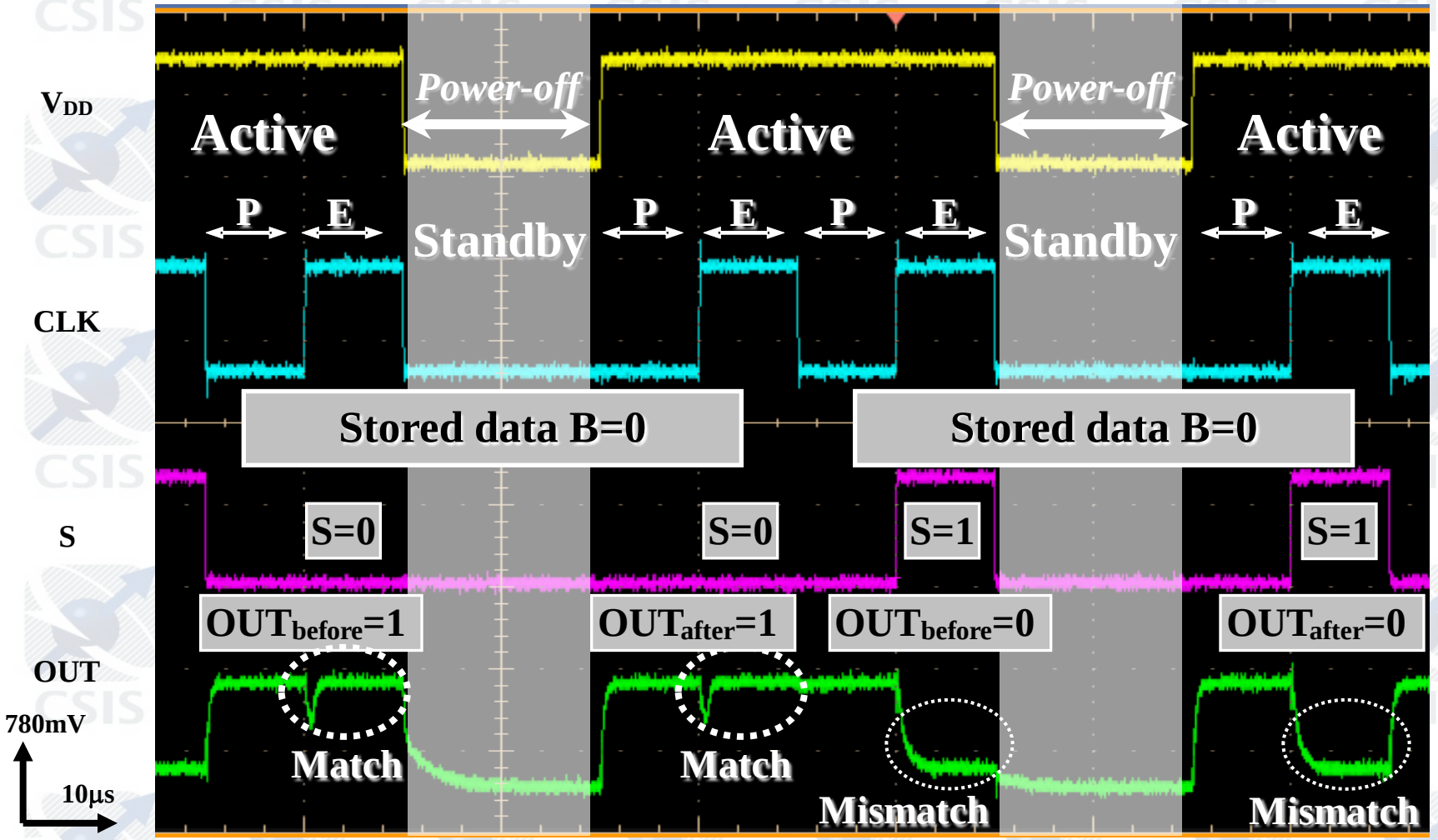
[b)] More high-speed write operation is possible with increase of write current. For example, with the average current of 327 μA at 10 ns write.

Waveforms of equality-search operations



Bit-level equality-search is successfully demonstrated.

Waveforms of sleep/wake-up operations



Instant sleep/wake-up behavior is successfully demonstrated.

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Conclusions

- Propose a **MOS/MTJ-hybrid** circuit (nonvolatile logic-in-memory circuit using MTJ devices) style
- Two kinds of typical applications with logic-in-memory architecture; **NV-LUT** circuit and **NV- TCAM**

⇨ Compact and no static power dissipation

- Confirm basic behavior with **fabricated test chips** under an MTJ/CMOS process.

⇨ It could open an **ultra-low-power** logic-circuit paradigm

Future Prospects and Issues:

1. Establish the fabrication line
2. Establish the CAD tools
3. Explore the appropriate application fields (Impact towards "**Reliability Enhancement**")