2nd Berkeley Symposium on
Energy Efficient Electronic Systems

November 3-4, 2011
Berkeley, CA, USA

# Nonvolatile CMOS Circuits Using Magnetic Tunnel Junction


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Work supported by the FIRST program of JSPS.

**http://www.csis.tohoku.ac.jp/**

# OUTLINE

- VLSI - challenges -
- Spintronics-based nonvolatile CMOS circuits
- Current status of magnetic tunnel junction
- Future directions
- Summary

# The FIRST Program

CSIS

Funding Program for World-Leading Innovative R&D on Science and Technology (30 Programs)

| | |
|---|---|
| Research Subject | "Research and Development of Ultra-low Power Spintronics-based VLSIs" |
| Core Researcher | Hideo Ohno, Prof. of Tohoku University |
| Program Planning & Selection | The Council for Science and Technology Policy |
| Program Management & Operation | Japan Society for the Promotion of Science(JSPS) |
| Program Duration | From FY 2009 through FY 2013 |
| Operational Support Institution | Tohoku University |
| Participating Institutions | Tohoku University, NEC, Hitachi, ULVAC<br>The University of Tokyo, Kyoto University<br>National Institute for Materials Science<br>Renesas Electronics, Covalent Silicon |

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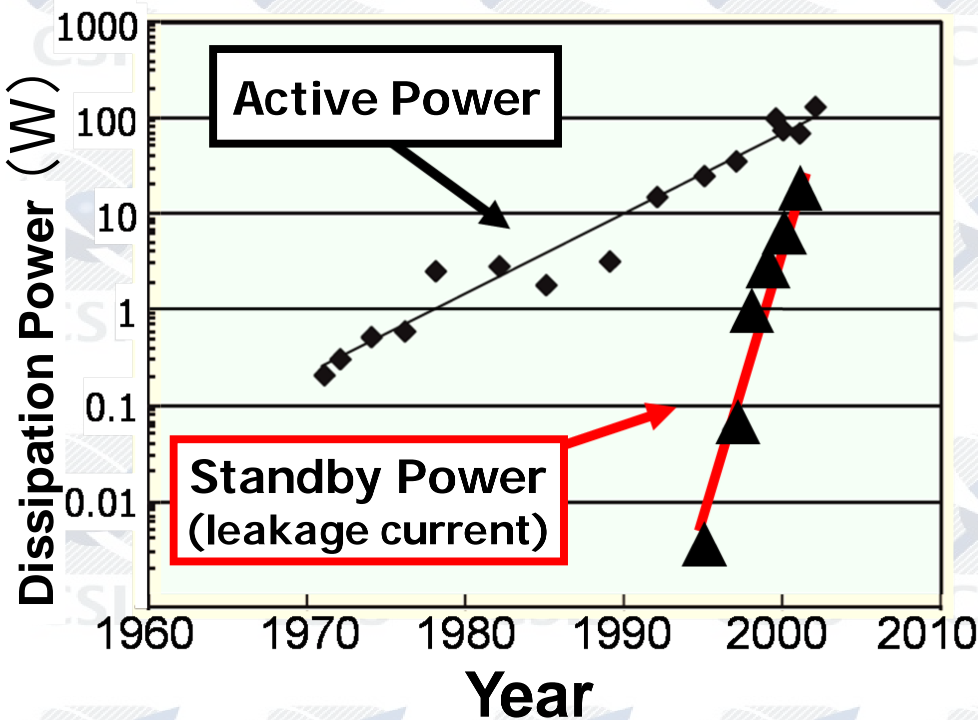
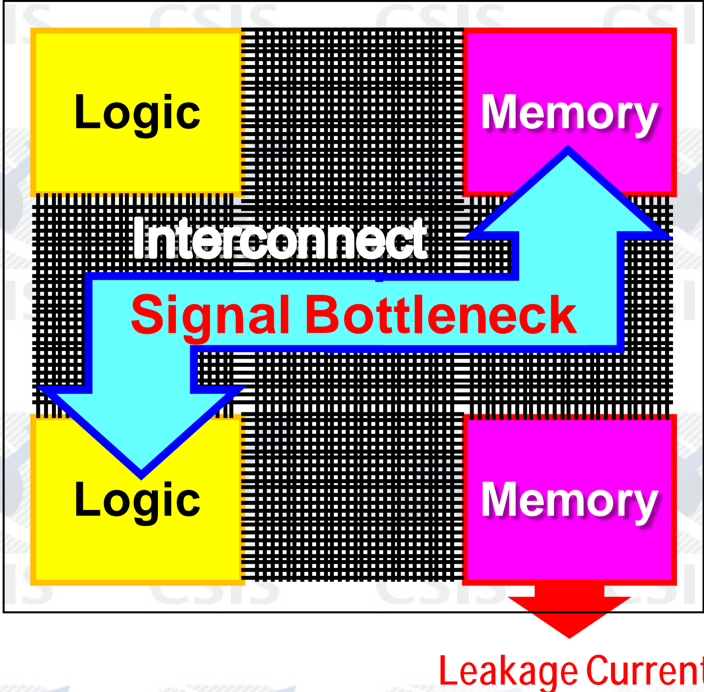
# Challenges Current VLSIs Face

## Power Consumption




## Interconnection Delay



# What do we need?

Nonvolatile memory that is

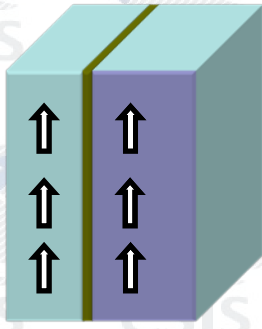
- scalable
- fast
- virtually infinite endurance
- back-end-of-line compatible

| Features of nonvolatile for memory device | NAND | FeRAM | Spin device |
|---|---|---|---|
| Access Speed | △ | ○ | ○ |
| Non destructive Read | ○ | △ | ○ |
| Write Endurance | × | △ | ○ |
| Scalability | ○ | △ | ○ |
| Operation voltage | × | △ | ○ |

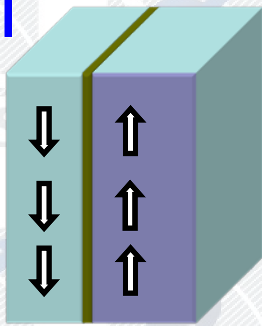
# Magnetic Tunnel Junction

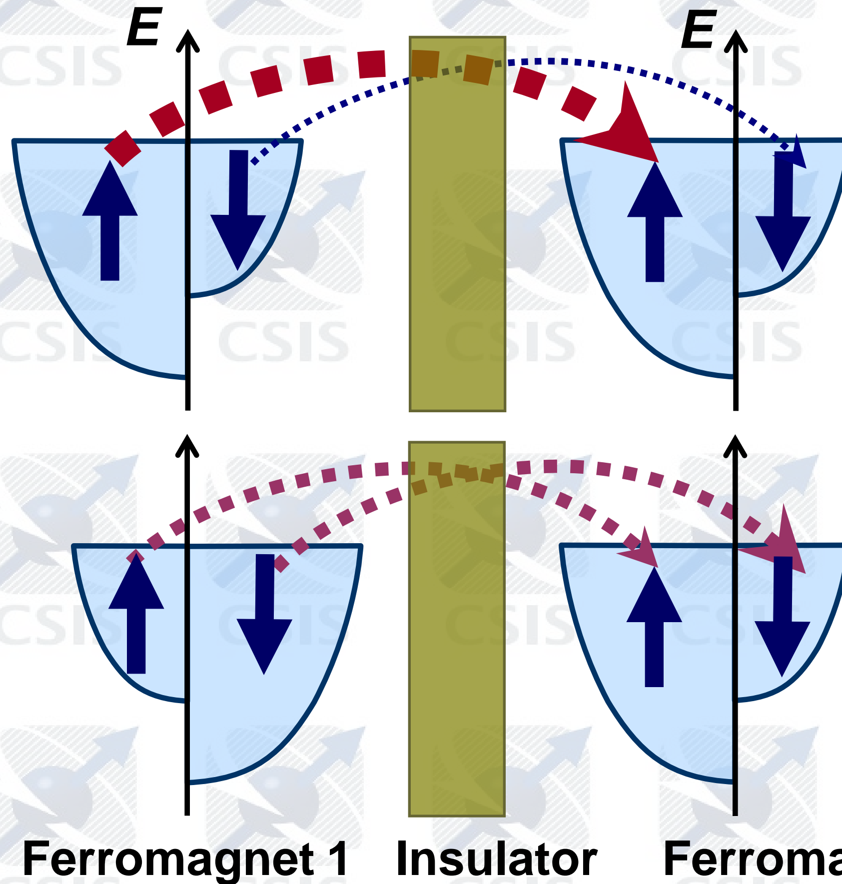
$$\text{Tunnel MagnetoResistance (TMR)} = \frac{R_{AP} - R_P}{R_P} = \frac{2P^2}{1 - P^2}$$

Parallel



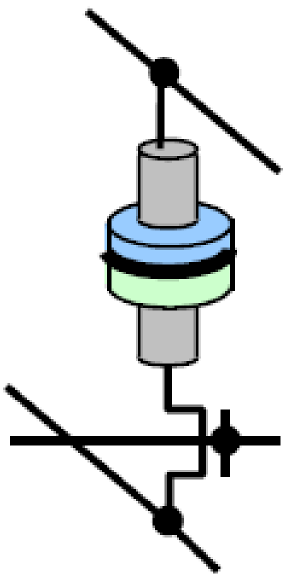
Antiparallel



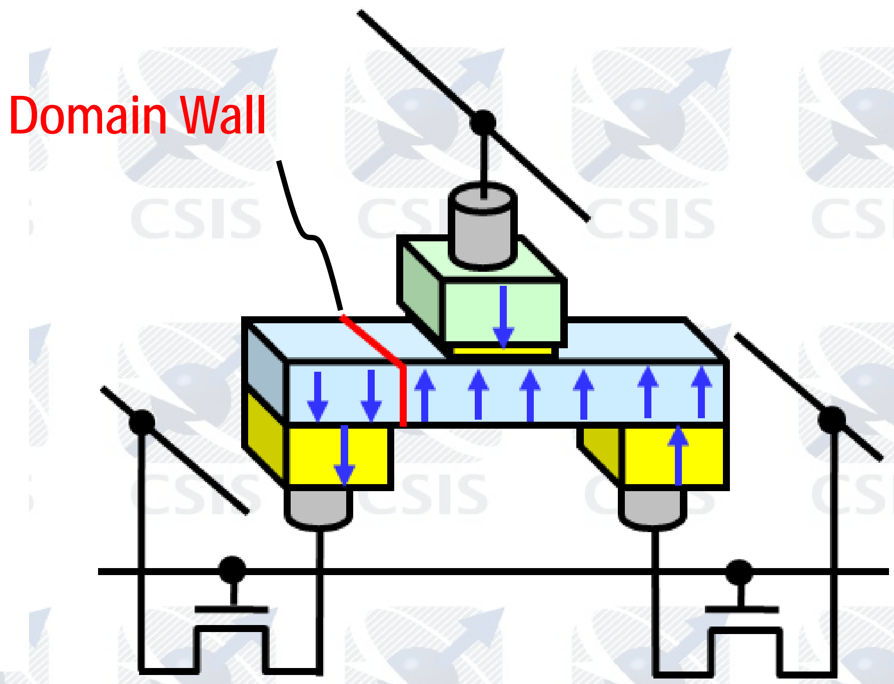



Room temperature TMR: Miyazaki and Tezuka (Tohoku U.), *J. Mag. Mag. Mat.* 1995 and Moodera *et al. Phys. Rev. Lett.* 1995.

# Magnetic Tunnel Junction Configurations



two terminal

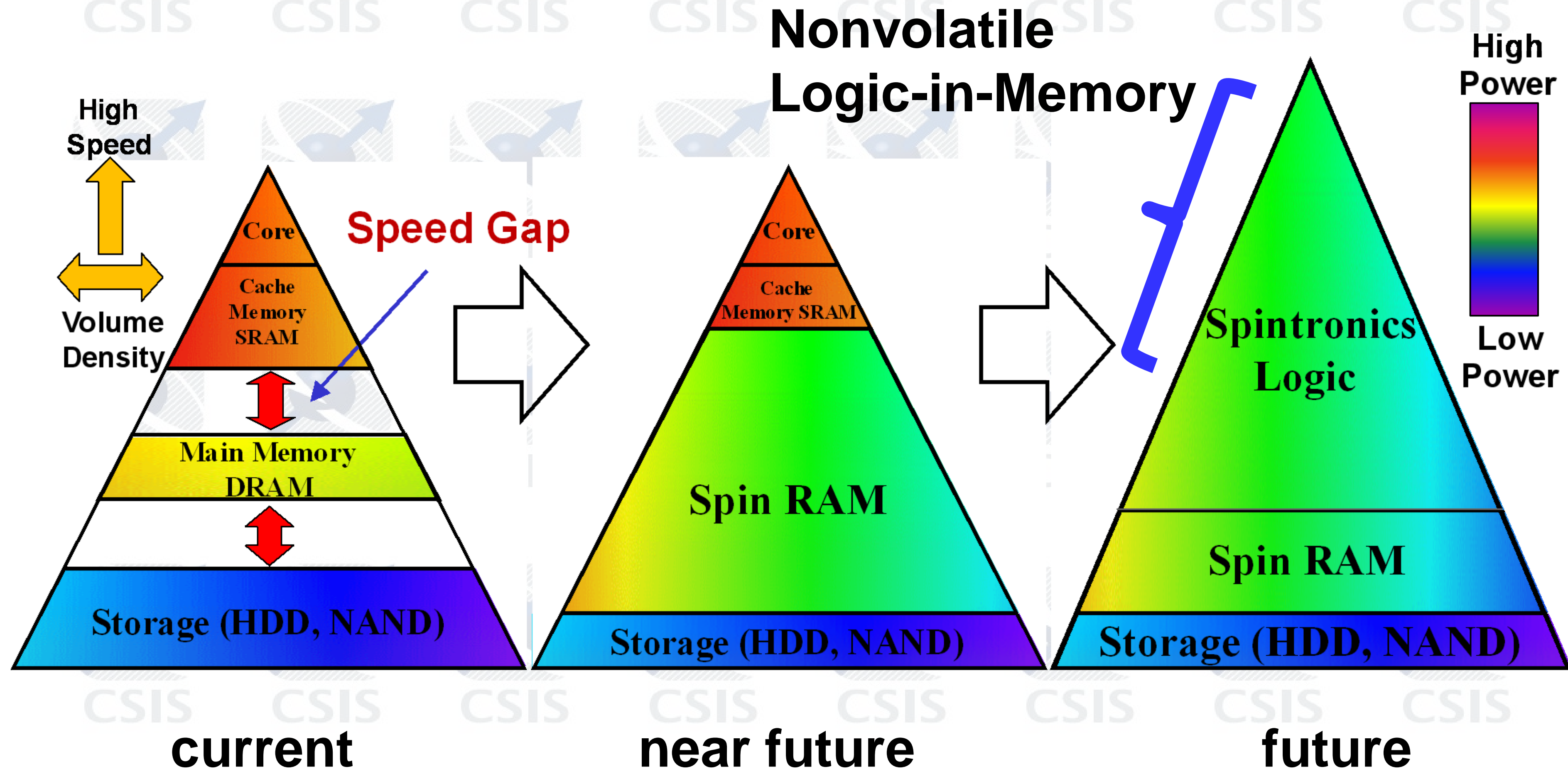



three terminal

**nonvolatile, fast and high endurance**

# Magnetic Random Access Memory

# System (Memory) Hierarchy




Magnetic tunnel junction based memory element to counter dynamic and static power, and interconnection delay

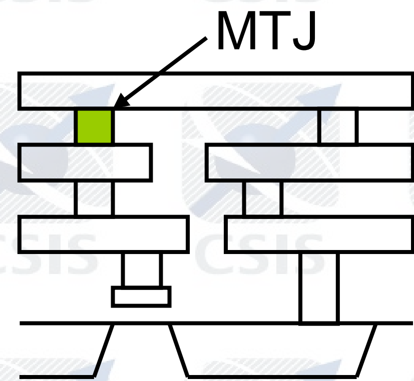
H. Ohno, E. Endoh, T. Hanyu, N. Kasai, and S. Ikeda (invited) IEDM 2010

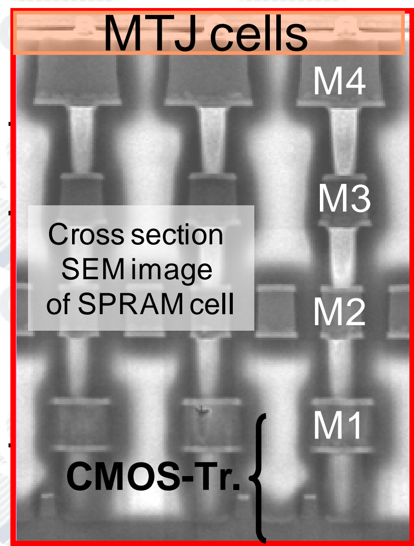
# Spintronics-based CMOS VLSI

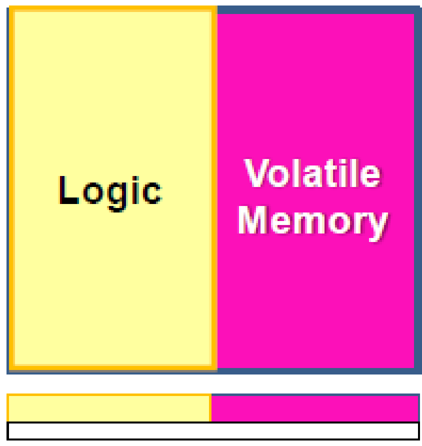
(1)Nonvolatile

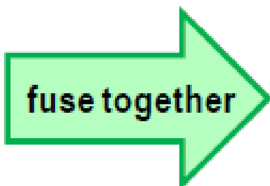
(2)Memory in the back end

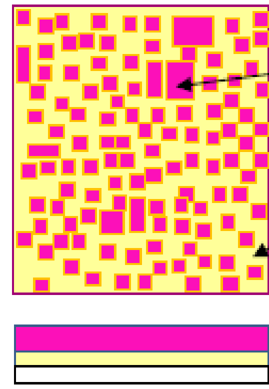
(3)Use of memory in processing



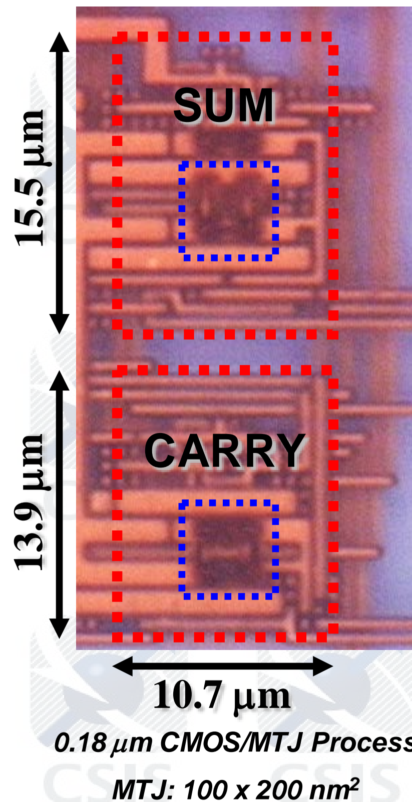



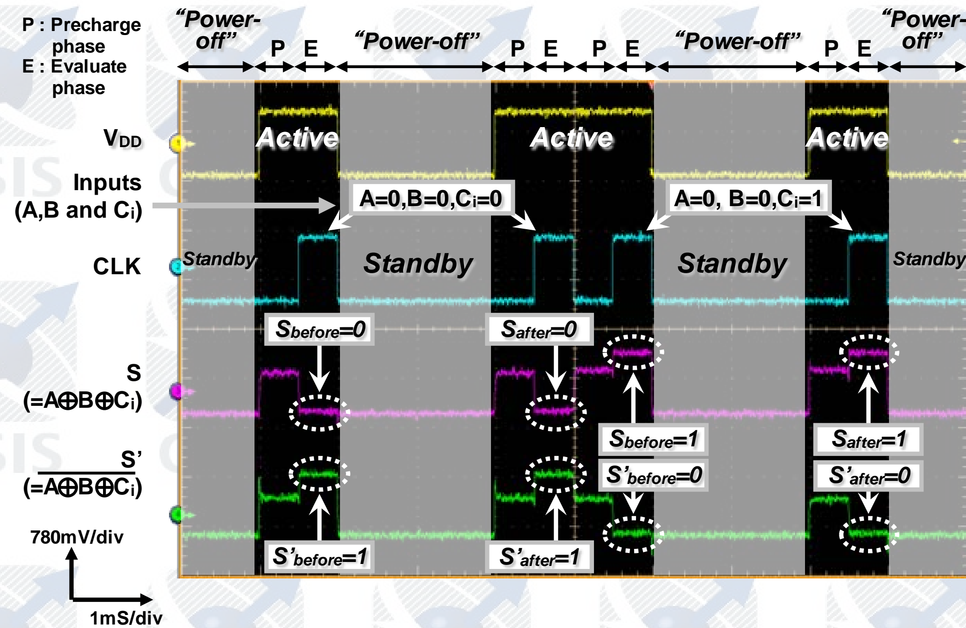
# Nonvolatile Logic-in-Memory

## Full adder block for image processing




*0.18 µm CMOS/MTJ Process*

*MTJ: 100 x 200 nm²*

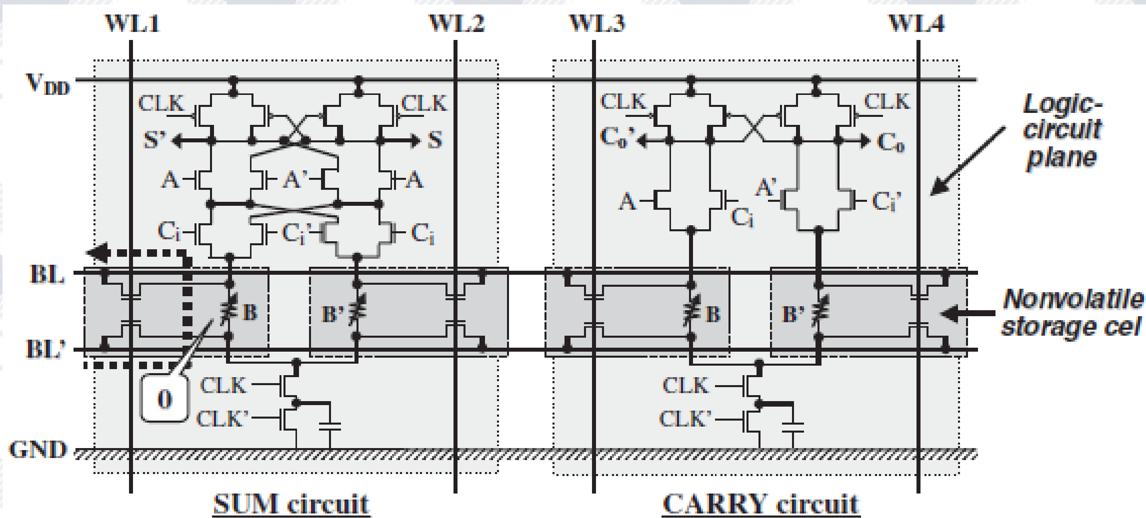



S. Matsunaga, … H. Ohno, T. Hanyu, APEX, 1, 091301 (2008)

Nonvolatile: **ultimate power gating** (no static power)

Memory in the back end + part of logic

(reduced # of tr. = suppression of delay and dynamic power)




## Full Adder Comparison

Simulation (except area/device #), 0.18 μm CMOS process

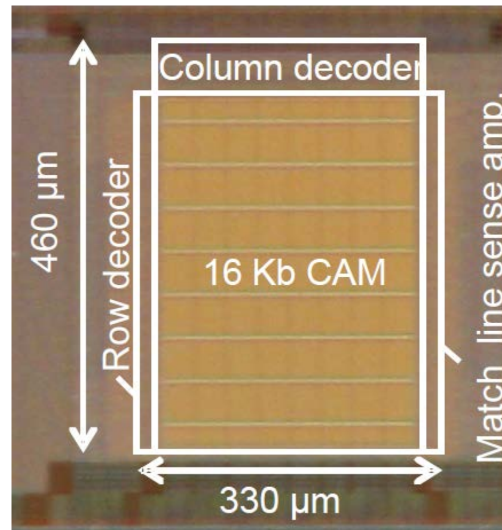
| | CMOS | CMOS/MTJ Hybrid |
|---|---|---|
| Delay | 224 ps | 219 ps |
| Dynamic power (@500 MHz) | 71.1 μW | 16.3 μW |
| Write time | 2 ns/bit | 10 ns/bit (2 ns/bit)[a)] |
| Write energy | 4 pJ/bit | 20.9 pJ/bit (6.8 pJ/bit)[a)] |
| Static power[b)] | 0.9 nW | 0.0 nW |
| Area (Device counts)[c)] | 333 $\mu m^2$ (42 MOSs) | 315 $\mu m^2$ (34 MOSs + 4 MTJs) |

**24% reduction in device count**

S. Matsunaga, … H. Ohno, T. Hanyu, APEX, 1, 091301 (2008)

# Nonvolatile CAM and TCAM

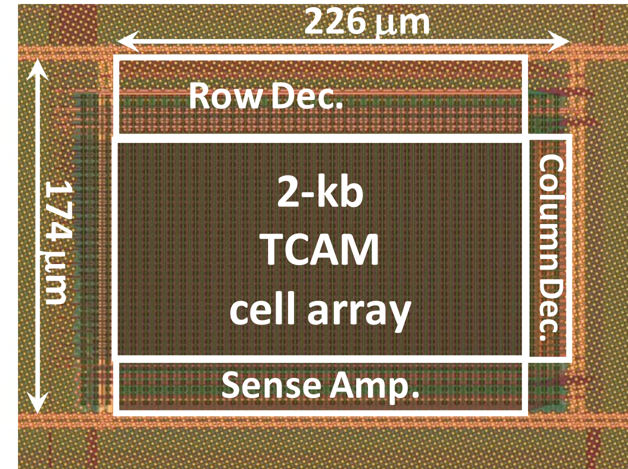
## Nonvolatile CAM




| Technology | 90 nm CMOS + DW Process |
|---|---|
| Cell size | 6.6 $um^2$/bit |
| Organization | 128 word x 128 bit |
| Supply voltage | 1.0 V |
| Search cycle time | 5 ns |

**Nebashi et al.**

## Nonvolatile TCAM




| Process | 90 nm 1P5M CMOS/MTJ |
|---|---|
| Cell structure | 6T-2MTJ |
| MTJ size | 100 nm x 200 nm |
| Cell size | 10.35 $\mu m^2$ |
| Array configuration | 32bits x 64words |
| Match delay | 0.29 ns |
| Supply voltage | 1.2 V |

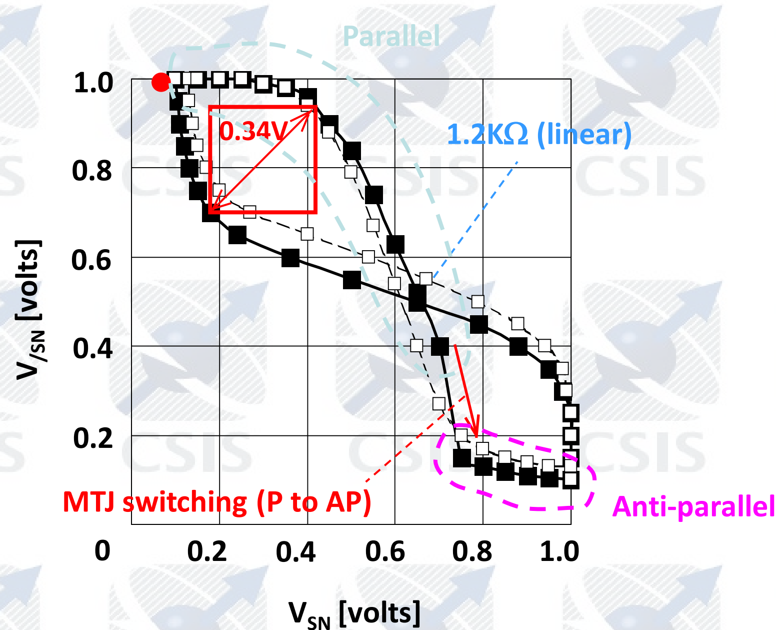
**Matsunaga et al.**

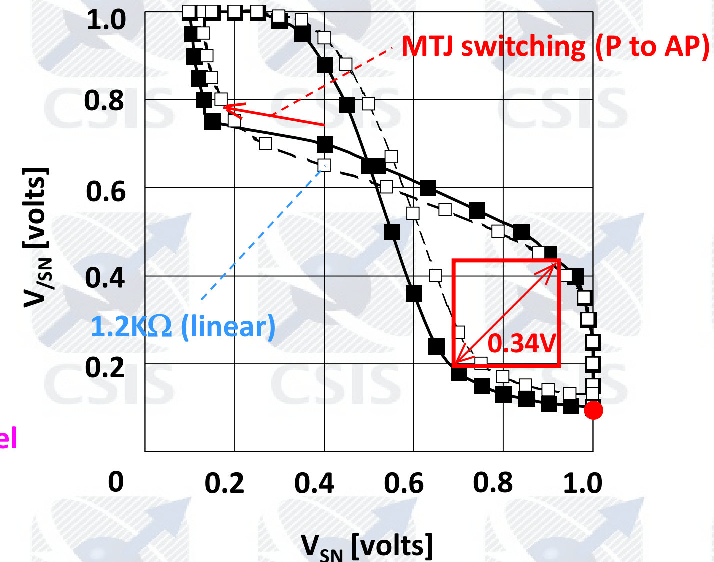
**VLSI Symp. 2011**

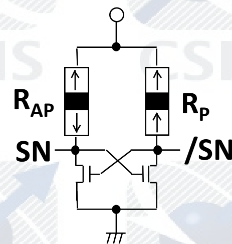
# Transfer curves of STT-SRAM cell

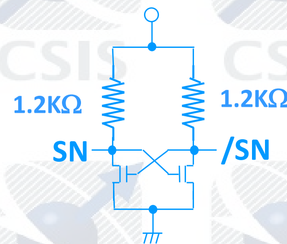
(a) “0” data latch

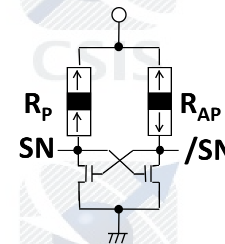
(b) “1” data latch




T. Ohsawa et al., SSDM 2011

# MTJ for VLSI: A wish list

1. Small footprint (*F* nm)
2. High output (TMR ratio > 100%)
3. Nonvolatility ($\Delta = E/k_B T > 40$)
4. Low switching current ($I_{C0} < F$ μA)
5. Back-end-of-the-line compatibility (350 °C)
6. Endurance
7. Fast read & write
8. Low resistance for low voltage operation
9. Low error rate
10. Low cost

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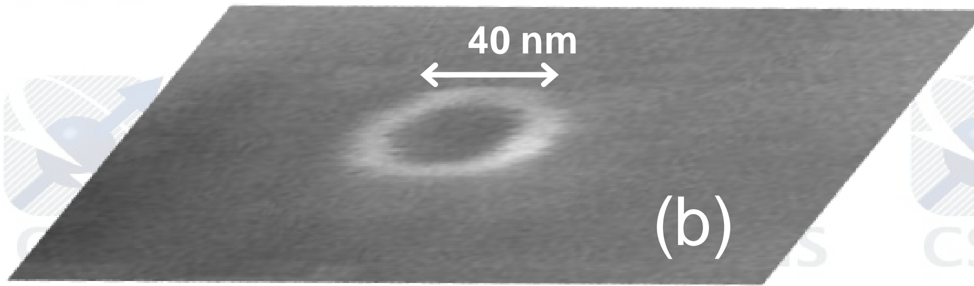
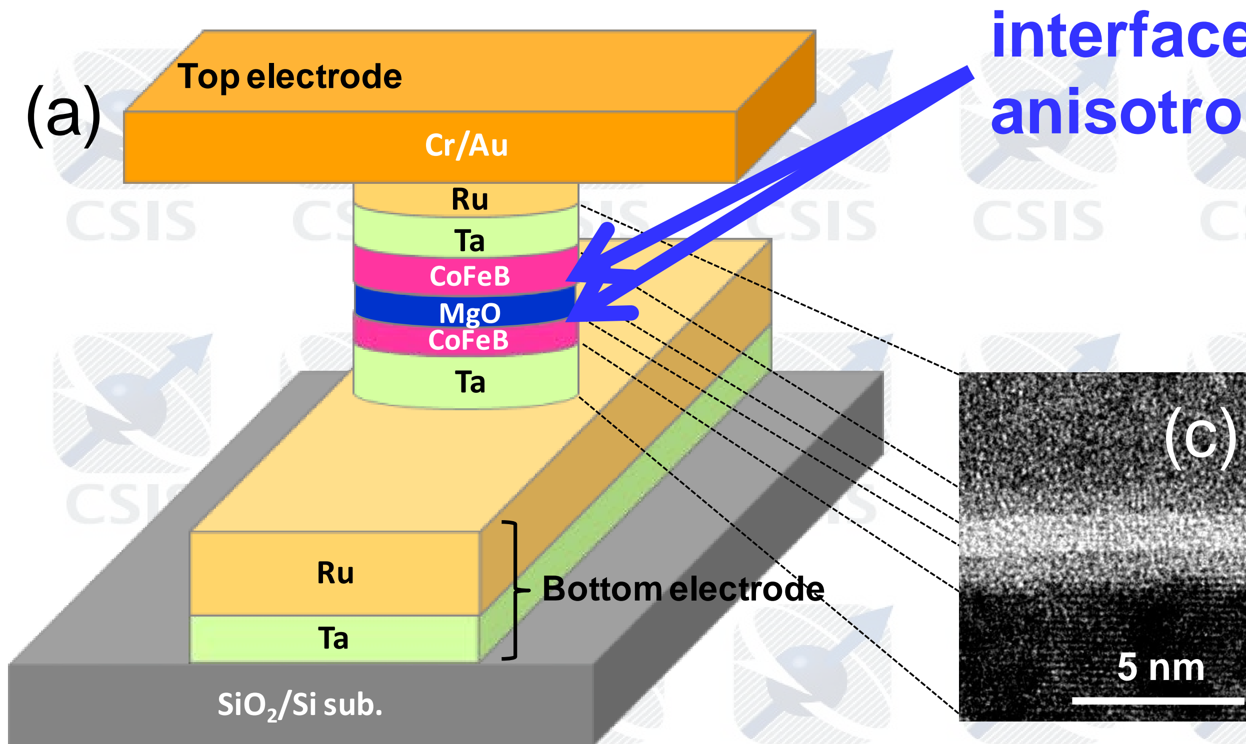
# Perpendicular MgO-CoFeB MTJ

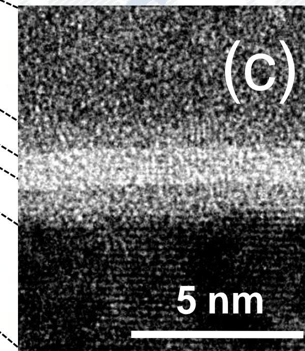
CSIS

$J_{C0}$ = 3.9 MA/cm$^2$
($I_{C0}$ = 49 μA)
$E/k_BT$ = 43
TMR ratio = 124%




interface perpendicular anisotropy



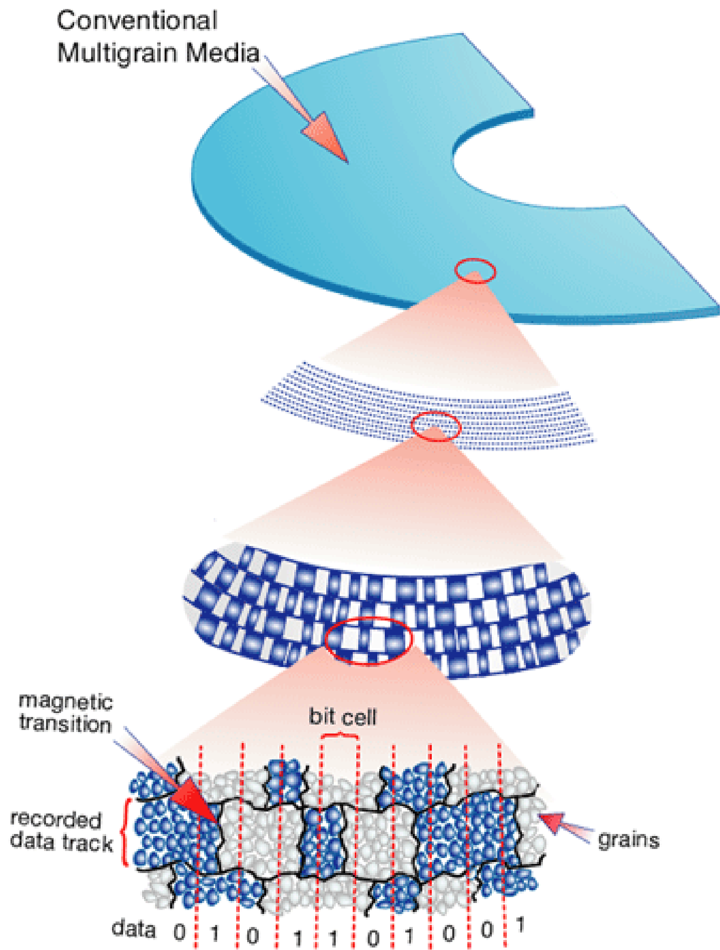



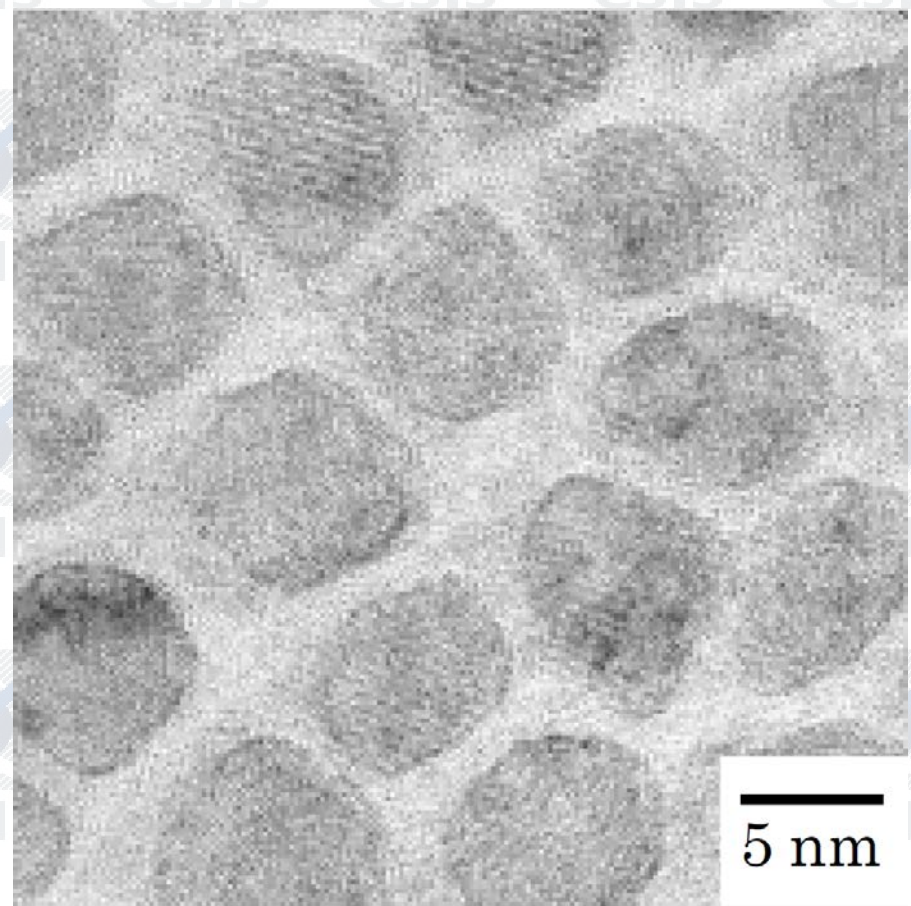

S. Ikeda et al., Nat. Mat. 9, 721 (2010), K. Miura et al., MMM 2010

# MTJ for VLSI: A wish list

| Wish | |
|---|---|
| 1. Small footprint (*F* nm) | 40 nm |
| 2. High output (TMR ratio > 100%) | 113% |
| 3. Nonvolatility ($E/k_B T$ >40) | 39 |
| 4. Low switching current ($I_C < F$ μA) | 48 μA |
| 5. Back-end-of-the-line compatibility (350 °C) | 350 °C |
| 6. Endurance | |
| 7. Fast read & write | |
| 8. Low resistance for low voltage operation | 16 Ωμm$^2$ |
| 9. Low error rate | |
| 10. Low cost | |

# How small can we go?



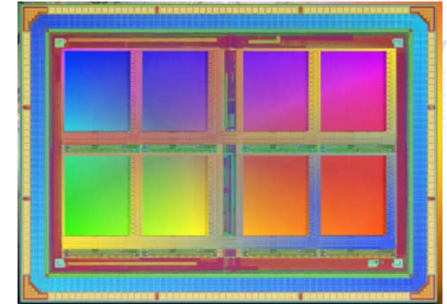

**CoPtCr-SiO2, Takei *et al.*, Fuji Electric review 55 (2009) 6..**

# Magnetization manipulation by

## Magnetic field

write/read heads for HDD
1st generation MRAM

http://www.hitachigst.com/

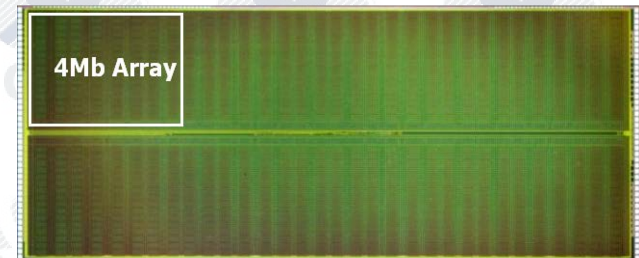


http://www.everspin.com/

## Spin current

L. Berger, J. Appl. Phys. **55**, 1954 (1984).
J. Slonczewski, J. Magn. Magn. Mat. **159**, L1 (1996).
L. Berger, Phys. Rev. B **54**, 9353 (1996).

Spin torque MRAM
Spin torque oscillator
Race-track memory




R. Takemura *et al*., VLSI Circ. Dig. p.84 (2009)

## Electric field

# Switching Energy

CSIS

## Spin-transfer switching

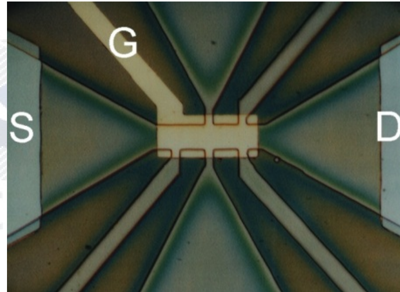
$$VIt = 0.5\ (\mathrm{V}) \times 30\ (\mu\mathrm{A}) \times 1\ (\mathrm{ns}) = 15\ (\mathrm{fJ})$$

## Electric field switching

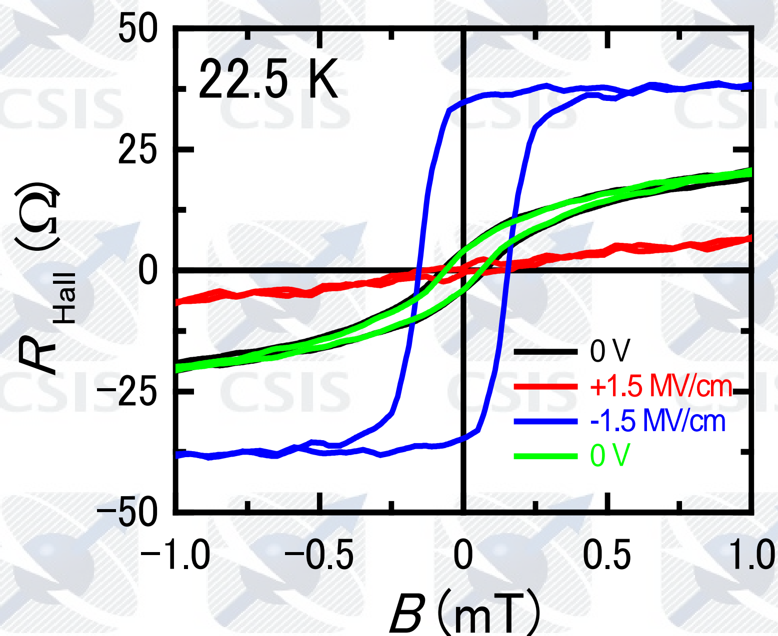
$$\begin{aligned} CV^2 &= \mathrm{S} \times \mathrm{d} \times \varepsilon \times \mathrm{E}^2 \\ &= \pi\left(\frac{30\ (\mathrm{nm})}{2}\right)^2 \times 5\ (\mathrm{nm}) \times 9.8\ \varepsilon_0 \times (5\ (\mathrm{MV/cm}))^2 \\ &= 0.08\ (\mathrm{fJ}) \end{aligned}$$

# Electric-field control of magnets

## Ferromagnetic transition

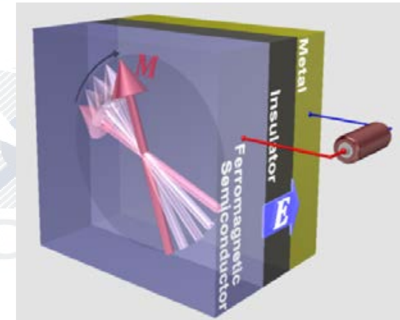



Ferromagnetic semiconductor (In,Mn)As

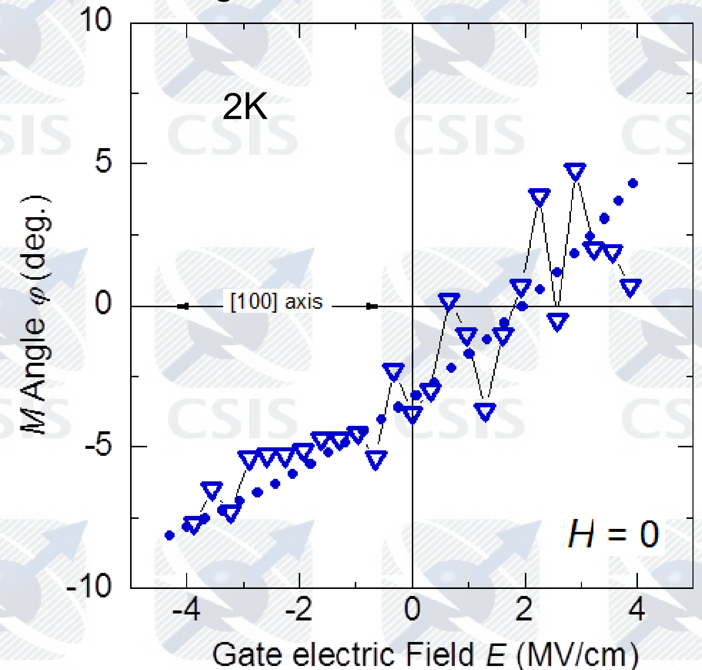



H. Ohno *et al.*, *Nature* 408, 944 (2000)

## Magnetization direction



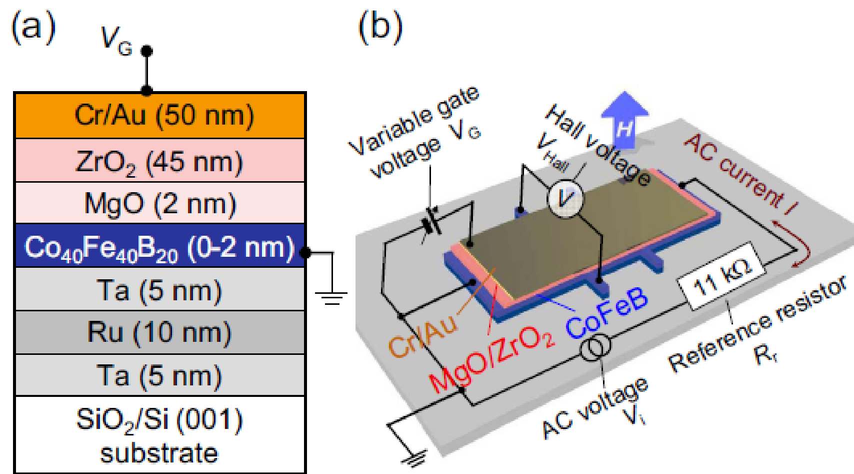

Ferromagnetic Semiconductor (Ga,Mn)As



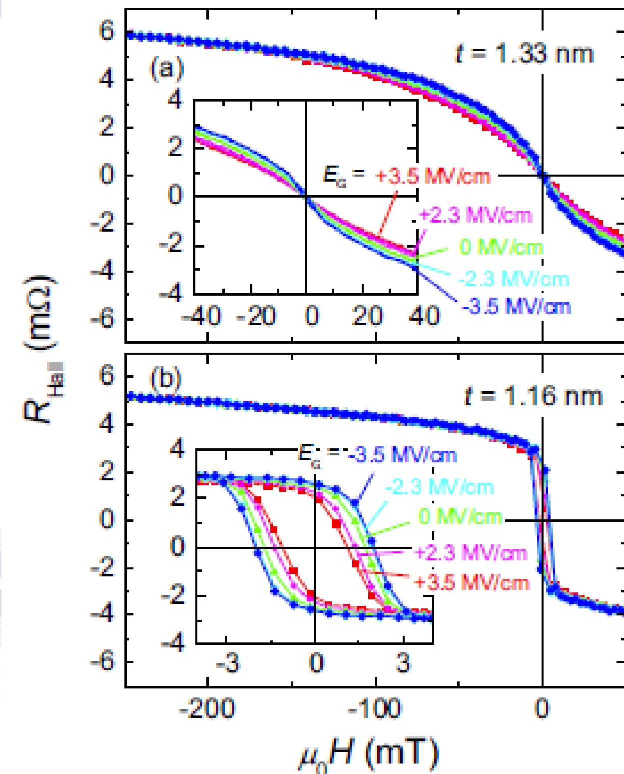

D. Chiba *et al.*, *Nature* 455, 515 (2008)

# Electric-field effects on CoFeB

## Manipulation of magnetic anisotropy in CoFeB at room temperature




M. Endo, et al. *Appl. Phys. Lett.* **96**, 212503 (2010).




See also; **FePt, FePd:** M. Weisheit *et al.*, Science (2007).

**Fe/Au:** T. Maruyama *et al.*, Nature Nanotechnology (2009).

# Summary

- Integrating spintronics nonvolatile memory element, magnetic tunnel junction, with CMOS realizes low-power, high performance, and stand-by power free nonvolatile VLSIs.
- Magnetic tunnel junction is much better positioned now than before with 30 nm dimension and beyond in sight. Once ready this could trigger a major paradigm shift.
- Electric field switching can realize ultra-low-power switching of magnetization.
- Spintronics may revolutionize the way VLSIs are made today.