

2013 Spintronics Workshop on LSI



June 10, 2013, 19:00 – 22:00
Rihga Royal Hotel Kyoto, Kyoto, Japan



General Information

The 2013 Spintronics Workshop on LSI will be held at Rihga Royal Hotel Kyoto, Kyoto, Japan, on June 10, 2013, just prior to the VLSI Symposium on Technology as a Satellite Workshop of the 2013 VLSI Symposia for the 3rd time. The workshop will focus on spintronics-based LSI technologies for high performance and ultra low power systems. Papers on current status, prospects and the remaining challenges in this field will be presented from invited speakers. The workshop is sponsored by Center for Spintronics Integrated Systems (CSIS), Tohoku University, which has been conducting the FIRST program supported by JSPS.

Registration

Advanced registration of the workshop will be available on the web site of the 2013 Symposia on VLSI Technology and Circuits (<http://www.vlsisymposium.org/>). The workshop fee is free of charge.

PROGRAM

Room : Kibune	
Opening 19:00 - 19:30	MTJ Technology: Materials and Performance Hideo Ohno (Tohoku University, Workshop Program Chair)
Invited talk 19:30 - 20:00	ST-MRAM Technology and Applications Jon Slaughter (Everspin Technologies)
Invited talk 20:00 - 20:30	Device Requirements for Scaled STT-MRAM Sung-Woong Chung (SK Hynix)
Invited talk 20:30 - 21:00	STT-MRAM and NV-Logic for Standby Power Zero Systems Tetsuo Endoh (Tohoku University)
Invited talk 21:00 - 21:30	STT-MRAM for Mobile SOC: Status and Outlook Seung Kang (Qualcomm)
Invited talk 21:30 - 22:00	MTJ-Based Nonvolatile Logic-in-Memory Architecture for Ultra-Low-Power VLSI Chips Takahiro Hanyu (Tohoku University)

Program Chair:

Hideo Ohno (Tohoku University),

Program Committee:

Hitoshi Wakabayashi (Tokyo Institute of Technology)

Philip Wong (Stanford University)

Tetsuo Endoh (Tohoku University)

Takahiro Hanyu (Tohoku University)

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