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*Tohoku University Develops World's First Fast Access Embedded
Memory that Stores Data without using Power*

Professor Tetsuo Endoh, Center for Spintronics Integrated Systems and Graduate School of Engineering, Tohoku University and a group led by Professor Hideo Ohno, Center for Spintronics Integrated Systems and Research Institute of Electrical Communication, Tohoku University, Sendai, Japan, have developed the world's first embedded memory that can transfer data as fast as today's state-of-the-art Static Random Access Memory (SRAM)¹ while maintaining its data even without power. This has been achieved by combining the magnetic tunnel junction (MTJ) technology that has been extensively researched in Tohoku University and state-of-the-art silicon technologies in an academic-industrial alliance with NEC Corporation, Tokyo, Japan. They succeeded in verifying the operating principle of the memory by measuring the 1Mb macro based on the MTJ fabrication technology developed in Tohoku University. They claim that this is a big leap toward lowering power consumption of today's LSIs, which are struggling for performance gain through miniaturization against increases in power.

The Endoh Laboratory of Tohoku University has developed new embedded memory macro that uses a magnetic tunnel junction (MTJ). The MTJ had been developed in spintronics technology where the interaction between electron's electrical charge and its quantum mechanical property, known as 'spin', play a crucial role in controlling the material's electrical features. The MTJ has two thin magnetic materials separated by a thinner dielectric film. The electrical current that flows through the sandwich structure changes depending on the relative direction of the spins in the two magnetic materials. The two different states, one with higher resistance and the other with lower resistance, are switched by applying voltage between the two magnetic materials in different directions, and the states maintain their characteristics even after removal of the voltage with virtually unlimited switching potential. The MTJ enables the memories, latches, and flip-flops² used in logic large-scale integrated circuits (LSIs) to be powered down without losing their stored data, the nonvolatile logic

LSI's being envisioned as a key device for the future super-low power electrical appliances.

Today's LSIs suffer from large power consumption as a consequence of transistor miniaturization, which is dominated by leak current flowing through off-state transistors during the standby state. The leak power in the SRAMs that are embedded in the LSIs constitutes the largest component, because more than half of today's LSI chip is occupied by the SRAMs on average. Therefore, the power saving in the embedded memories has been very eagerly awaited.

The developed 1Mbit nonvolatile embedded memory macro that is fabricated in 90nm CMOS/MTJ technologies satisfies both high-speed data access that is required in the LSI's logical computation and zero-power in the standby state. Furthermore, its macro size can be smaller than the conventional SRAM one when the memory is designed and fabricated in the state-of-the-art manufacturing process technologies, which is attractive given the trend of memory amount increase in the future system LSIs.

Key features of these new developed technologies are as follows:

i) High-speed access and zero standby power

The high-speed data access is achieved through the world's fastest 1.0ns wake-up time, which is the time needed for loading data stored in the MTJ to a memory cell circuit. This fast wake-up time is made possible by a fine-grained power-gating technique³ where power-on/off control is performed for a 32-bit-cell grain.

ii) Higher memory density than SRAM

The memory cell consists of four transistors and two MTJs that are placed on the transistors, its cell size being determined by the four transistors alone. Since the conventional SRAM consists of six transistors, the memory cell size of the developed memory becomes smaller than the SRAM. This is a big advantage, especially for the future system LSIs that are to have large memories embedded.

iii) Stable data retention at low power supply voltages

The static noise margin (SNM) that stands for an index to judge the SRAM cell's stability in holding data against device parameter fluctuation in the manufacturing process is shown to increase automatically due to the resistance switching of the MTJs used in the memory cell. This is an advantage at low power supply voltage over the conventional SRAM cell, which is becoming more unstable in holding data as device size shrinks.

Tohoku University and NEC are developing nonvolatile logic LSIs using MTJs to achieve super low-power LSIs. The achievement of this nonvolatile embedded memory macro marks a step forward to realizing the goal by making LSIs standby-power-free while maintaining

their trend of performance increase when it is combined with the development of nonvolatile logic LSIs.

Tohoku University and NEC will announce their latest results on June 13 at the 2012 Symposium on VLSI Technology (June 12-15, Hawaii, USA).

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(notes)

1. SRAM

SRAM stands for static random access memory, which is commonly embedded in logic LSIs. The data are stored in a circuit with six transistors, and their access time is fast enough to be synchronized with the logic data processing speed. The data are destroyed after power down (volatile).

2. Latches and flip-flops

The latch is a unit to store one-bit data in synchronization with a signal, and the flip-flop is formed by combining the two latches to constitute a commonly used circuit for storing data in current mainstream LSIs' data processing.

3. Power-gating technique

A circuit technology in which power supply is stopped for a block of circuits during its standby state to eliminate the leak power consumed in the off-state transistors. The grain is the power control unit. The fine-grained power gating is effective for power reduction, because the time becomes short when the power is supplied to a circuit during standby.

For inquiries:

Naoki Kasai, Deputy Director

Center for Spintronics Integrated Systems, Tohoku University

TEL: +81-22-217-6115

E-mail: n-kasai@csis.tohoku.ac.jp