June 11, 2012

Tohoku University

Standby-Power-Free Large-Scale Integrated Circuits using Nonvolatile Spintronics Devices
- Now with high speed, density, and reliability -

[Abstract] A research group of Professor Hideo Ohno of Center for Spintronics Integrated Systems and Research Institute of Electrical Communication of Tohoku University together with NEC Corporation (NEC) developed a standby-power-free spintronics[1]-based large-scale integrated circuit (LSI) using a nonvolatile magnetic tunnel junction (MTJ), a spintronic device. The developed LSI technologies are (1) fast access and high density nonvolatile core memory embedded in logic LSIs, (2) nonvolatile ternary content addressable memory (TCAM), (3) error correction circuits for highly reliable logic LSIs, (4) three-dimensional chip stack for nonvolatile logic LSIs, and (5) a reliable three-terminal spintronics device. They will be presented at the 2012 IEEE VLSI Symposia held at Honolulu, Hawaii on June 12-15, 2012.

[Background]

A logic integrated circuit, where intelligent systems are integrated on a single chip die, is a key modern technology that determines the quality of various systems as well as infrastructures. A paradigm shift of technology has occurred whenever the power consumption of logic LSIs has reached a limit by increasing the level of integration and speed. Recently, standby power consumption in logic VLSIs has become as large as operation power consumption, which calls for an innovation that enables ultra-low standby power to further enhance VLSI performance. Standby-power-free operation can be achieved by nonvolatile data retention in logic LSIs where power supply can be cut off wherever in the chip whenever it is not in operation. A spintronics device composed of a magnetic tunnel junction is currently the only nonvolatile memory candidate for this purpose, because of its high-speed, low-voltage, and non-destructive operation together with virtually infinite read/write endurance.

[Research program]

Under the project "Research and Development of Ultra-low Power Spintronics-based VLSIs" (core researcher: Hideo Ohno), which started in March 2010 and is granted by the Japan Society for the Promotion of Science (JSPS) through the “Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program),” initiated by the Council for Science and Technology Policy (CSTP), the center aims at assuming a leading role in achieving innovative change by the fusion of spintronic devices and logic integrated circuits. In this way, the center purposes to play a pivotal role in the world-wide innovation cycle of logic VLSIs.

The center concurrently promotes the research and development of spintronics materials, devices, and circuits. In doing this, it aims to establish an inimitable technology structure for spintronics logic integrated circuits that includes research and development, processing and production technology, and circuit design as well as a circuit integration prototyping environment. Furthermore, the center plans to demonstrate the high performance of spintronics logic integrated circuits at ultra-low power that far surpasses the conventional levels as well as a high-performance ultra-low power integrated computing system that combines processing and memory through logic-in-memory architecture using nonvolatile spintronics memories and CMOS. An open innovation center for spintronics logic integrated circuits will be established at the center, creating a standard for high-performance ultra-low power systems. Through these dynamic processes, the center plans to play a critical role in educating and training researchers and engineers, giving hands-on knowledge of all the aspects of spintronics-based VLSIs.

[Presenting contents]

Tohoku University together with NEC developed the following circuit designs and device technology for standby-power-free spintronics-based LSIs that combine a high level of integration and high speed.

(1) "The World's First Fast Access Embedded Memory that Stores Data without using Power."

(2) "The World's Smallest Cell Implementation for a High-density Standby-Power-Free TCAM in combination with Silicon/Magnetic Devices."

These LSIs were designed using 90-nm CMOS technology by Tohoku University, and the embedded spintronics device was fabricated on a 300-mm wafer[2].

NEC together with Tohoku University developed the world's first nonvolatile spintronics-based logic circuits with redundancy for spintronics-based system LSIs, which are highly reliable logic LSIs.

(3) "Groundbreaking New Technology for Improving the Reliability of Spintronics Logic Integrated Circuits."

Tohoku University developed the world's first three-dimensional stacked spintronics-based logic chip for ultrafast parallel reconfiguration in system LSIs.

(4) "The World's First 3-D Reconfigurable Spin Logic Chip with Spintronics Technology."

Tohoku University together with Kyoto University and NEC demonstrated the world's first three-terminal spintronics device that has high reliability with sufficient operation stability, high endurance, and 10-years' nonvolatile data retention at a temperature of 150°C.

(5) "The first demonstration of highly reliable spintronics devices."

For inquiries:

Naoki Kasai, Deputy Director

Center for Spintronics Integrated Systems, Tohoku University

TEL: +81-22-217-6115

E-mail: n-kasai@csis.tohoku.ac.jp

Notes:

1. Spintronics

Spintronics, also known as magnetoelectronics, is an emerging technology that exploits two features of an electron, both the intrinsic spin of the electron and its associated magnetic moment, in addition to its fundamental electronic charge, in solid-state devices, such as magnetic devices and electron devices. Electronics equipments have been developed drastically by both higher-density data storage magnetic devices (hard disk) and higher-speed electron devices (semiconductor integrated circuits) independently. Spintronics has been expected as breakthrough technology for future ultra-low-power and high-speed integrated circuits, which will lead to zero-standby power electronics equipment.

2. 300-mm wafer fabrication

Spintronics devices were fabricated on a 300-mm wafer using the Super Clean Room (SCR) in Tukuba Innovation Arena (TIA).