2011 Spintronics Workshop on LSI



June 13, 2011 Rihga Royal Hotel Kyoto, Kyoto, Japan



General Information

The 2011 Spintronics Workshop on LSI will be held at Rihga Royal Hotel Kyoto, Kyoto, Japan on June 13, 2011, just prior to VLSI Symposium on Technology of the VLSI Symposia for the first time. The workshop will focus on spintronics-based LSI technologies for high performance and ultra low power systems. The six papers will be presented from invited speakers. The workshop is sponsored by Center for Spintronics Integrated Systems(CSIS), Tohoku University, which has been conducting the FIRST program supported by JSPS.

Registration

Advanced registration of the workshop will be available on the web site of 2011 Symposia on VLSI Technology and Circuits (http://www.vlsisymposium.org/). Workshop fee is free.

PROGRAM

Room: Suzaku II (Kibune) 2F	
Opening Remarks: Spintronics for Nonvolatile Electronics	
Hideo Ohno (Tohoku University, Workshop Chair)	
Recent Progress and Emerging Technology of Spintronics	
Device for VLSI	
Jean-Pierre Nozieres (Spintec)	
Challenges in Non-volatile Etch	
Joydeep Guha (Lam Research)	
Technology, Manufacturing and Markets of	
Magnetoresistive Random Access Memory (MRAM)	
Brad Engel (Everspin Technologies)	
Advances in Materials and Structures for STT-RAM	
Vladimir Nikitin (Grandis)	
Embedded Spintronics Integrated Circuits for	
System-on-Chips	
Seung Kang (Qualcomm)	
MTJ-Based Nonvolatile Logic-in-Memory Architecture	
Takahiro Hanyu (Tohoku University)	

Titles of the five invited talks will be announced on CSIS web page (http://www.csis.tohoku.ac.jp/english/index.html).

Program Chairs: Hideo Ohno (Tohoku University), Tetsuo Endoh (Tohoku University)

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Secretariat: Secretariat for VLSI Symposia (Japan), c/o ICS Convention Design, Inc.

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