CoFeB/MgO based perpendicular magnetic tunnel junctions with stepped structure for symmetrizing different retention times of "0" and "1" information

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Outline

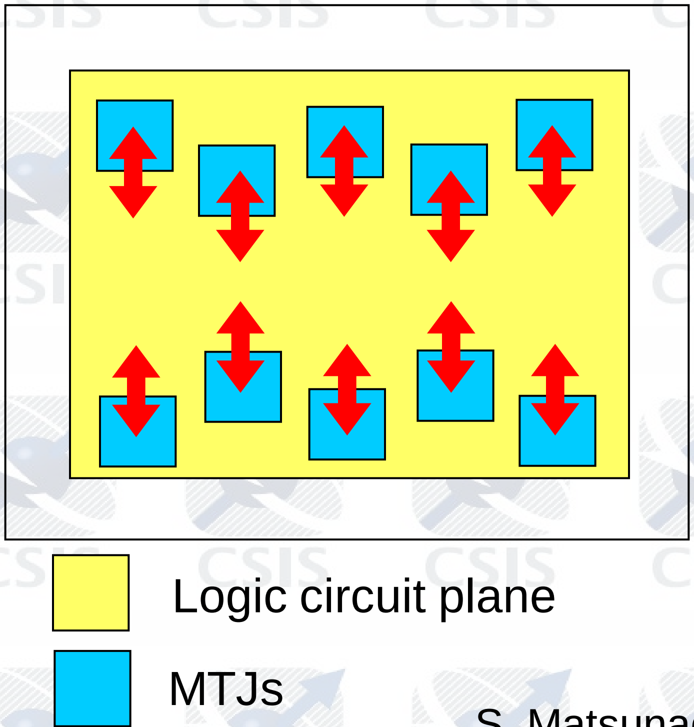
- Background
- Issue of perpendicular magnetic tunnel junctions (p-MTJs)
- Proposal of p-MTJs with stepped structure
- Fabrication and characterization of stepped structure
- Cell area of stepped structure
- Proposal of self-alignment process
- Summary

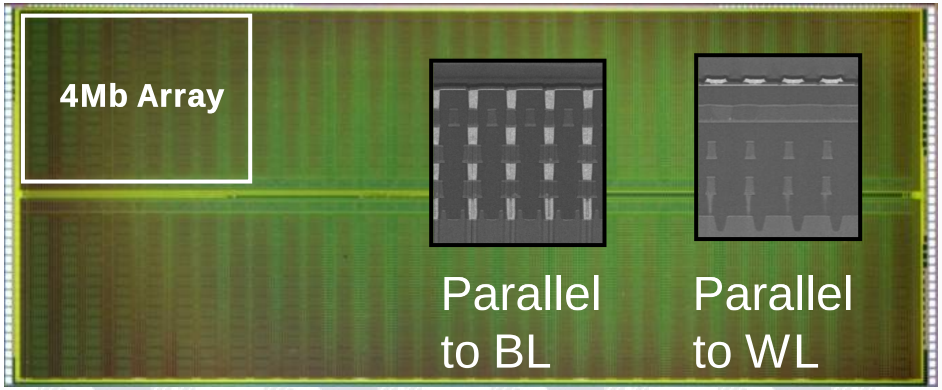
Background

- Applications using MTJs as memory elements.

Logic-in-memory VLSI

STT-RAM

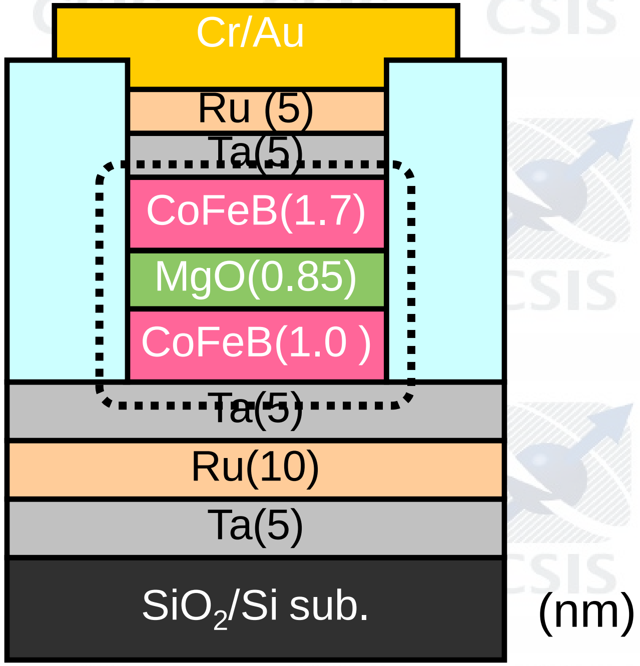




S. Matsunaga *et al*., Appl. Phys. Express **1**, 091301 (2006).
R. Takemura *et al*., VLSI Circ. Dig. pp.84-85, (2009)

Advantages of perpendicular MTJs

- We successfully developed CoFeB/MgO based perpendicular MTJ (p-MTJ).



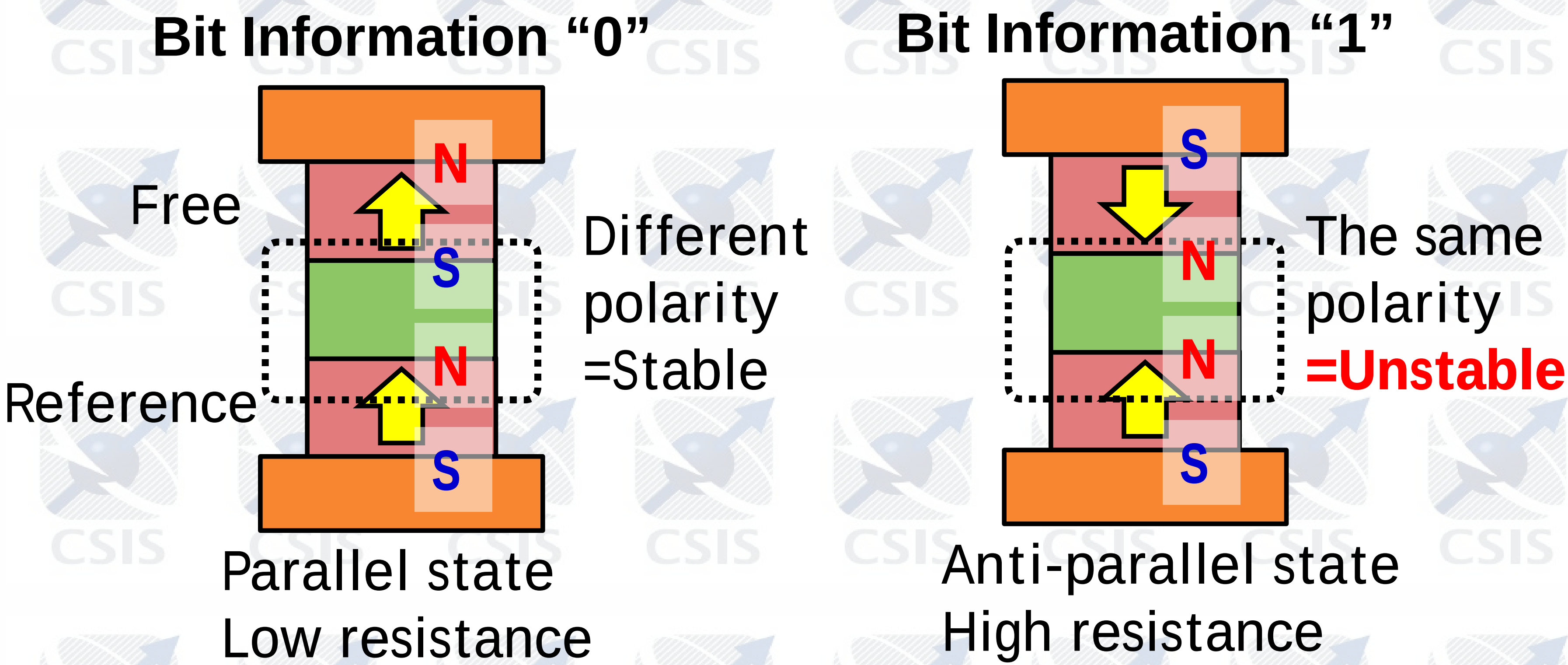
Requirements for applications

1. High TMR ratio
2. Low switching current
3. High thermal stability factor
4. Back-end-of-line compatibility

S. Ikeda *et al.*, Nature Mater. **9**, 721 (2010).
K. Miura *et al.*, Abstract for 55th MMM conference, HC-02, (2010).

Issue for p-MTJs

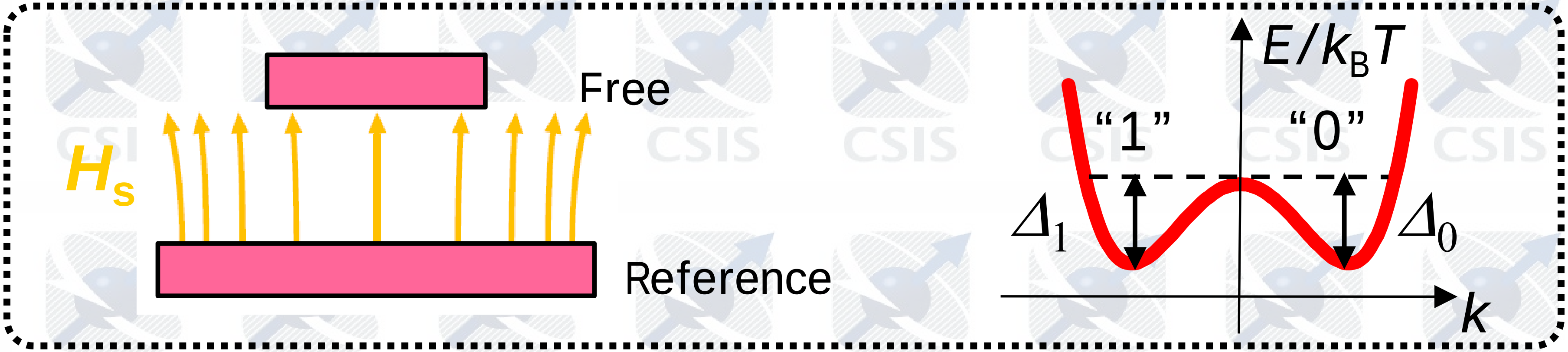
- Different stability between states storing “0” and “1” information.



Reduction of thermal stability

- Δ_1 increases with increasing diameter of reference layer.

$$\Delta_{0,\,1} = \Delta\,[1 \pm H_s / H_{c0}]^2$$

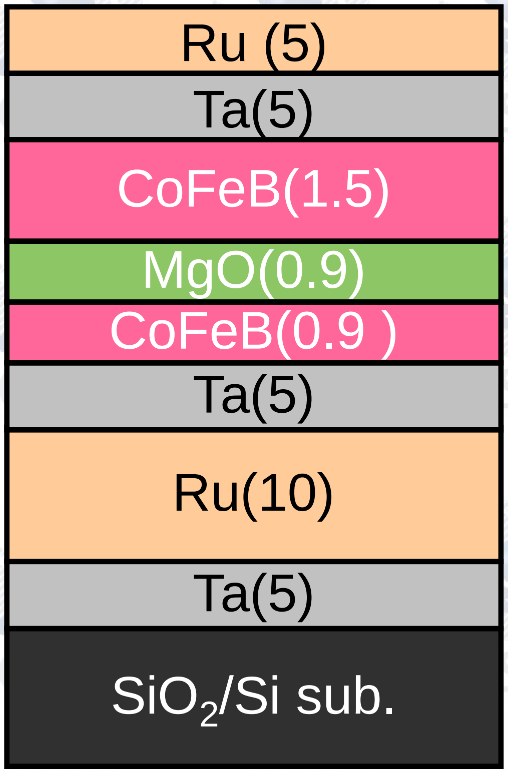


Objectives

- Symmetrizing different retention times of "0" and "1" information.
  - ◆ Development of p-MTJ with stepped structure for suppressing reduction of Δ_1.
  - ◆ Verification of advantage of stepped structure over conventional structure.

Sample preparation

- $Co_{20}Fe_{60}B_{20}$ ferromagnetic layers and MgO tunnel barrier combination are used.



Stacked structure

<u>Deposition</u>

- RF magnetron sputtering @RT
- Gas pressure : Ar 0.1-0.4 Pa
- Cathodes :4”ϕ

<u>Fabrication</u>

- EB and Photo lithography
- Ar-ion milling

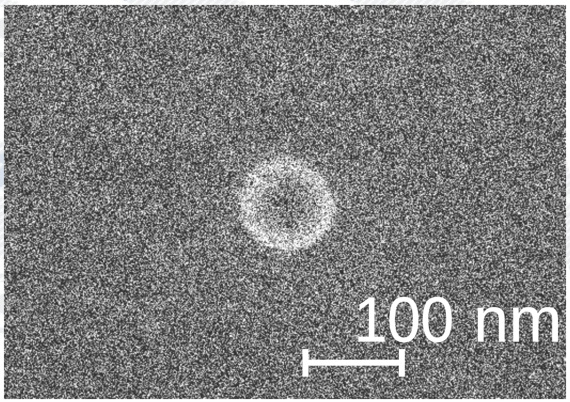
<u>Post annealing</u>

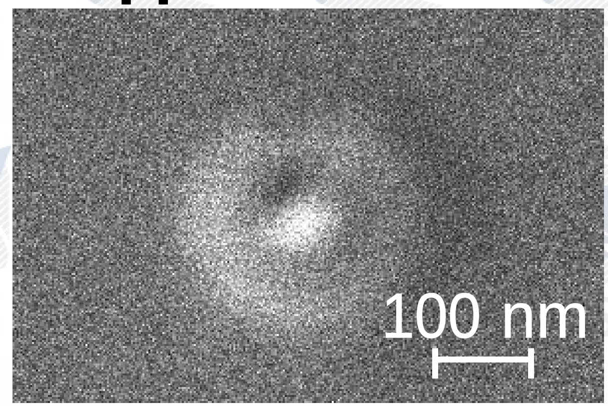
- 300ºC
- H=400 mT (perpendicular)

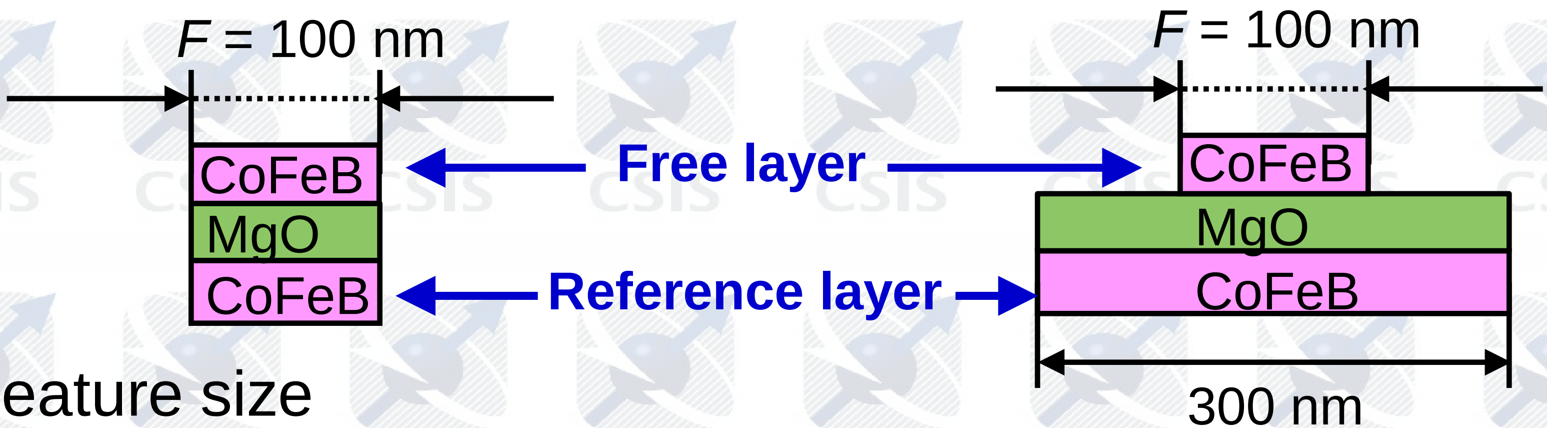
Two types of p-MTJs

- We fabricated two types of MTJs which have same feature size.

Conventional structure **Stepped structure**



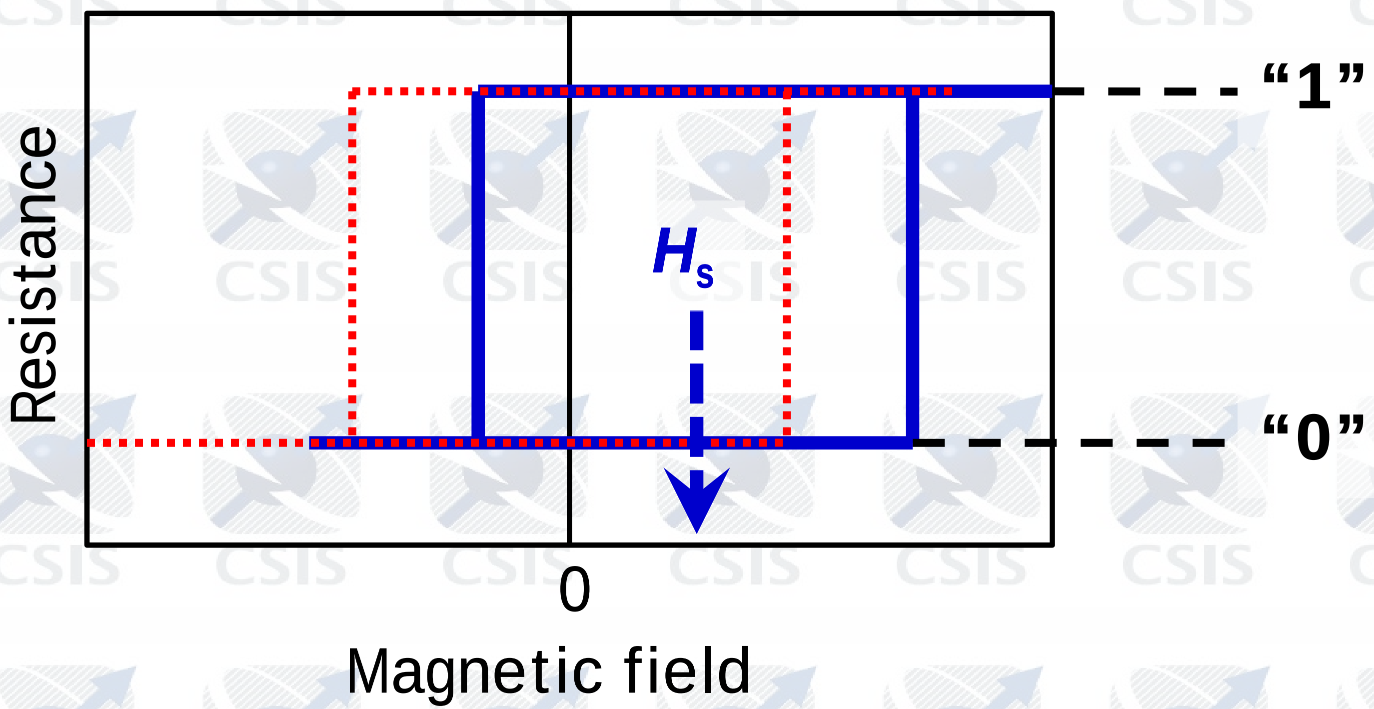




F : Feature size

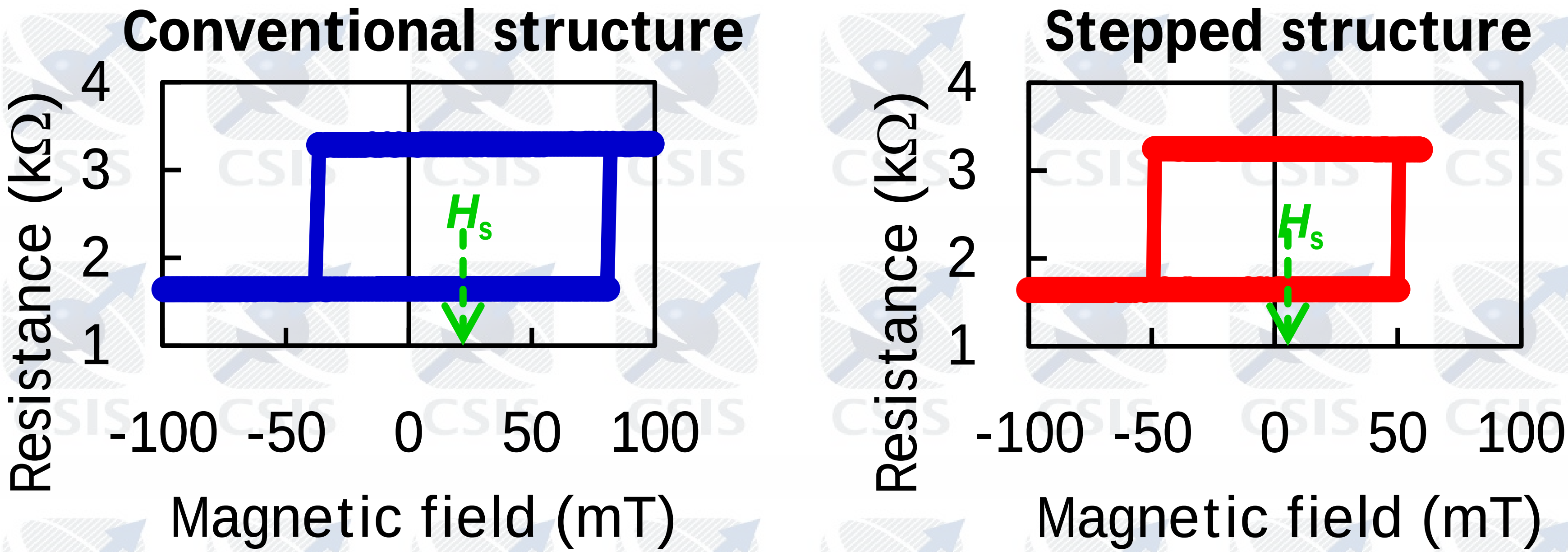
Method to determine H_s experimentally

- H_s can be determined from shift of hysteresis loop with respect to H=0.



H_s in two types of p-MTJs

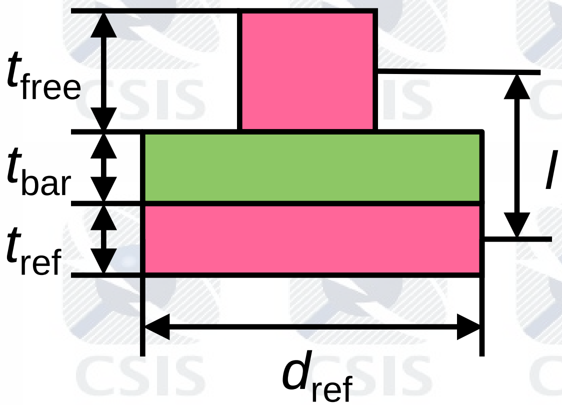
- H_s can be reduced by using stepped structure.



	Conventional structure	Stepped structure
TMR ratio (%)	100	97
RA (Ωμm²)	13	13
H_s (mT)	22	5

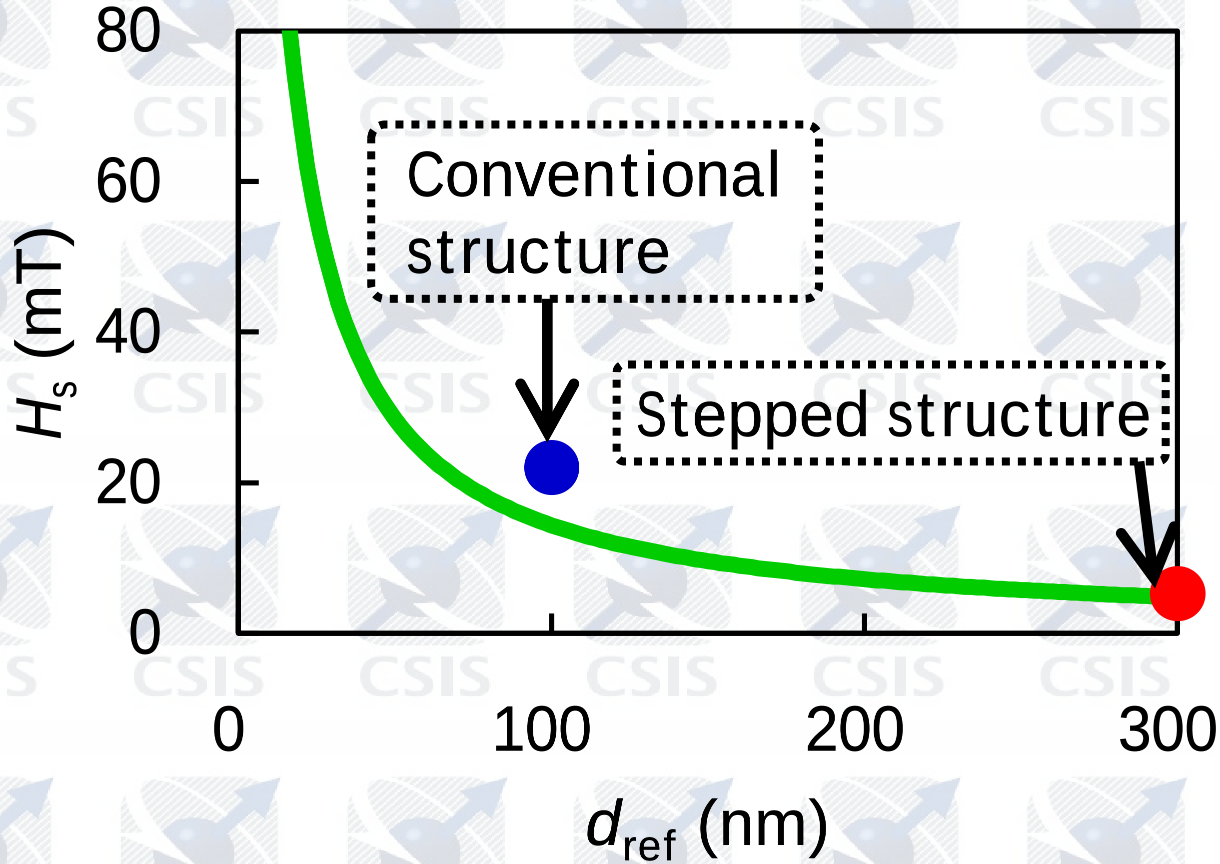
Experimental and estimated H_s

- Experimental results are roughly agreed with the calculation curve.



$$H_s = \frac{M_s t_{ref} \left(\frac{d_{ref}}{2}\right)^2}{2\mu_0 \left[\left(\frac{d_{ref}}{2}\right)^2 + l^2\right]^{\frac{3}{2}}}$$

$$l = t_{free}/2 + t_{ref}/2 + t_{bar}$$



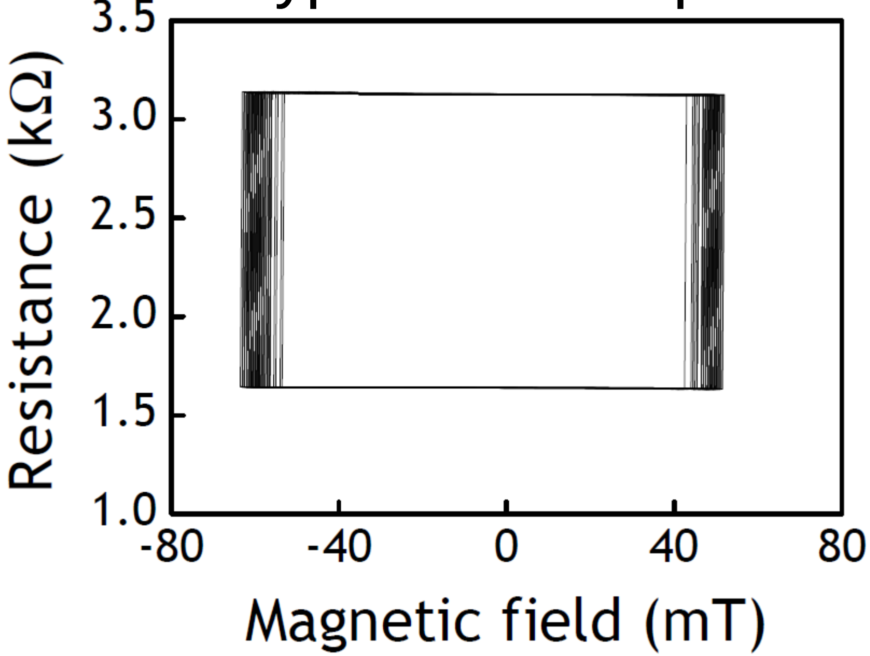
Method to determine Δ_0 and Δ_1

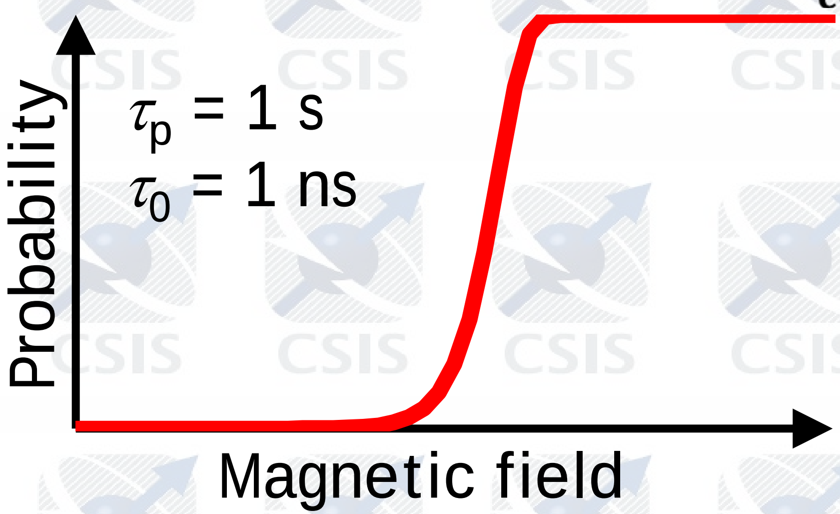
- We measured resistance as a function of magnetic field 100 times to obtain switching probability.

$$\text{Probability} = 1 - \exp\left\{1 - \frac{\tau_p}{\tau_0}\exp\left[\Delta\left(1 - \frac{H - H_s}{H_{c0}}\right)^2\right]\right\}$$

$$\Delta_{0,1} = \Delta\left(1 \pm \frac{H_s}{H_{c0}}\right)^2$$

Typical *R*-*H* loops

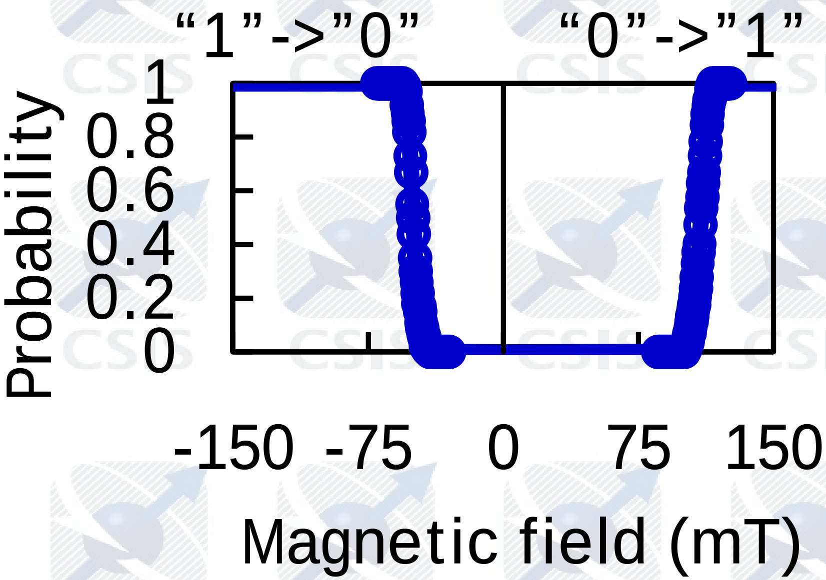




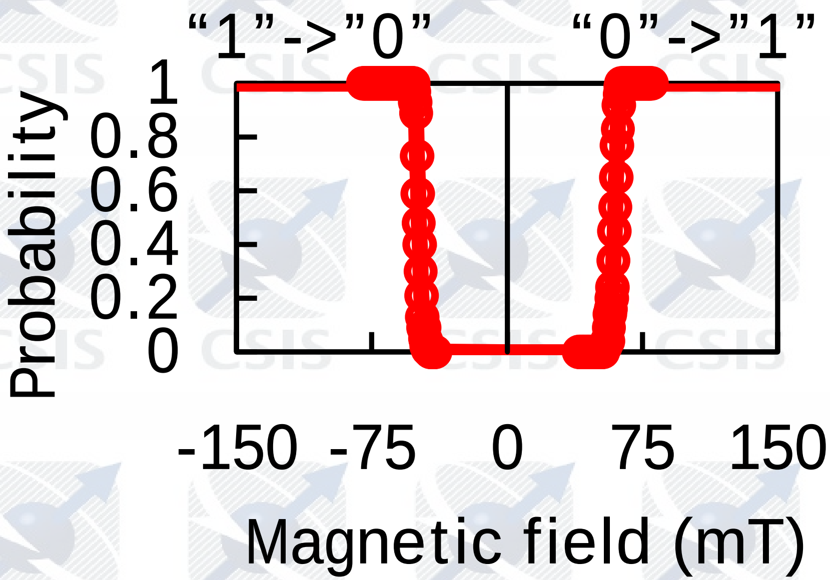
Δ_0 and Δ_1 in two types of p-MTJs

- Δ_0 and Δ_1 in stepped structure are almost equivalent.

Conventional structure



Stepped structure



	Conventional structure	**Stepped structure**
Δ_0	71.2	72.9
Δ_1	46.5	70.1

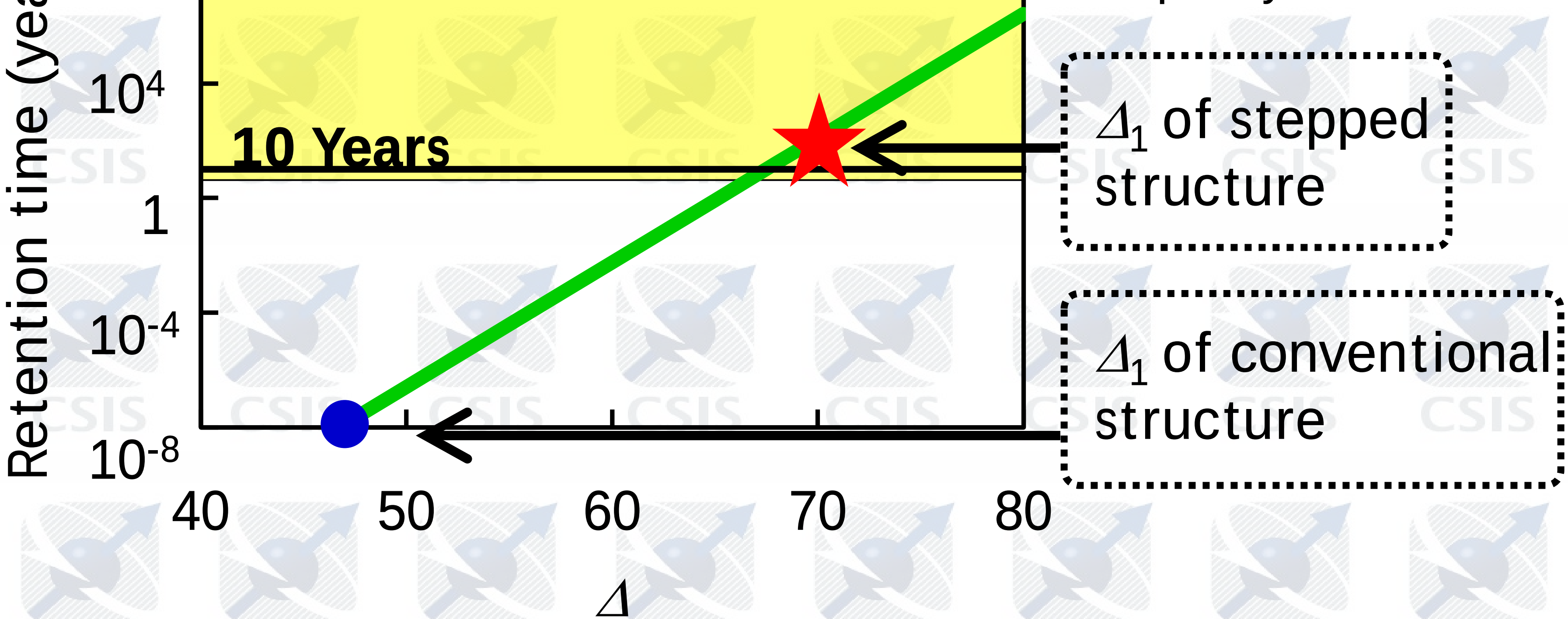
Retention time and Δ_1

- Retention time over 10 years is achieved by employing stepped structure.

$$\text{retention time} = -\frac{t_0 \ln(1 - P_{\text{chip}})}{n \exp(-\Delta)}$$

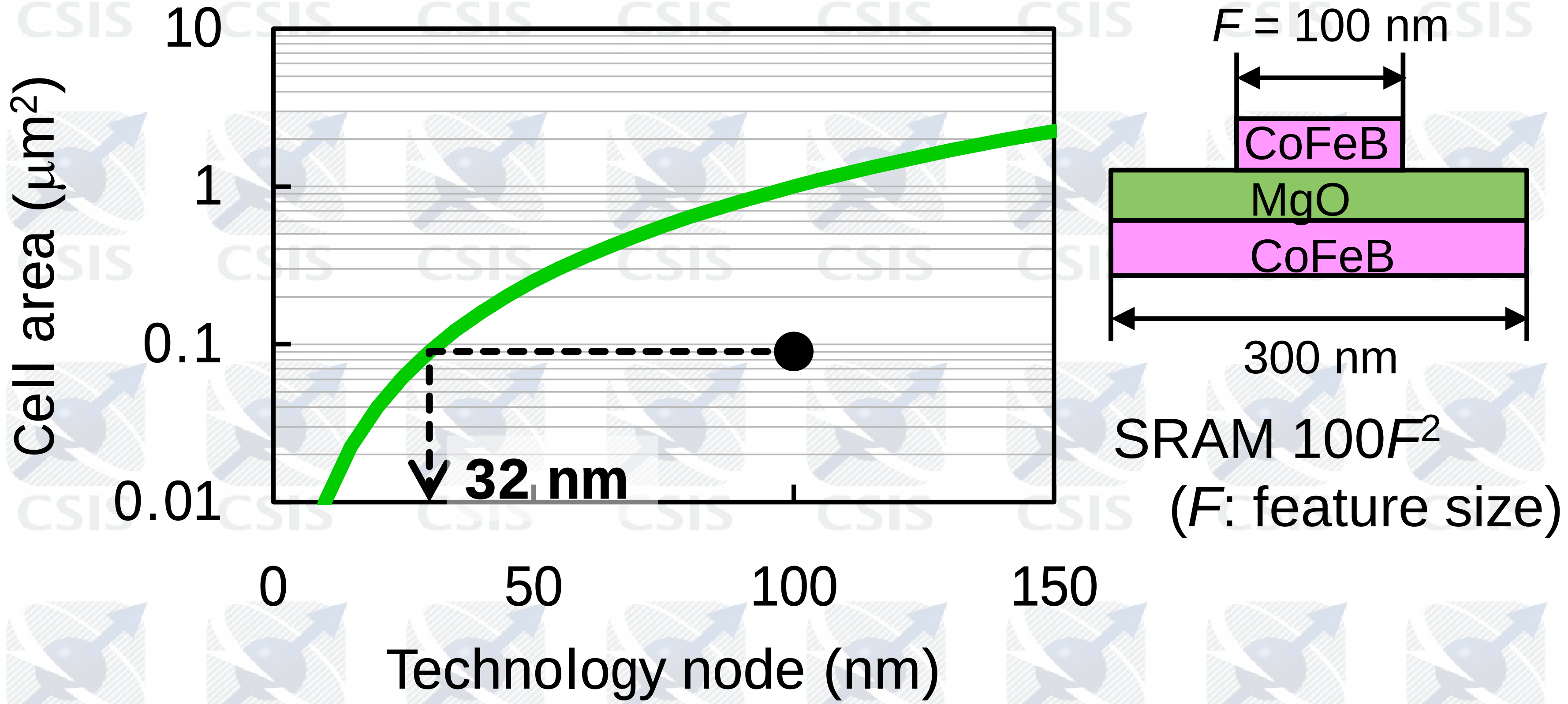
Chip error rate P_{chip} : 10^{-4} for 10 years

Capacity n : 64Mb



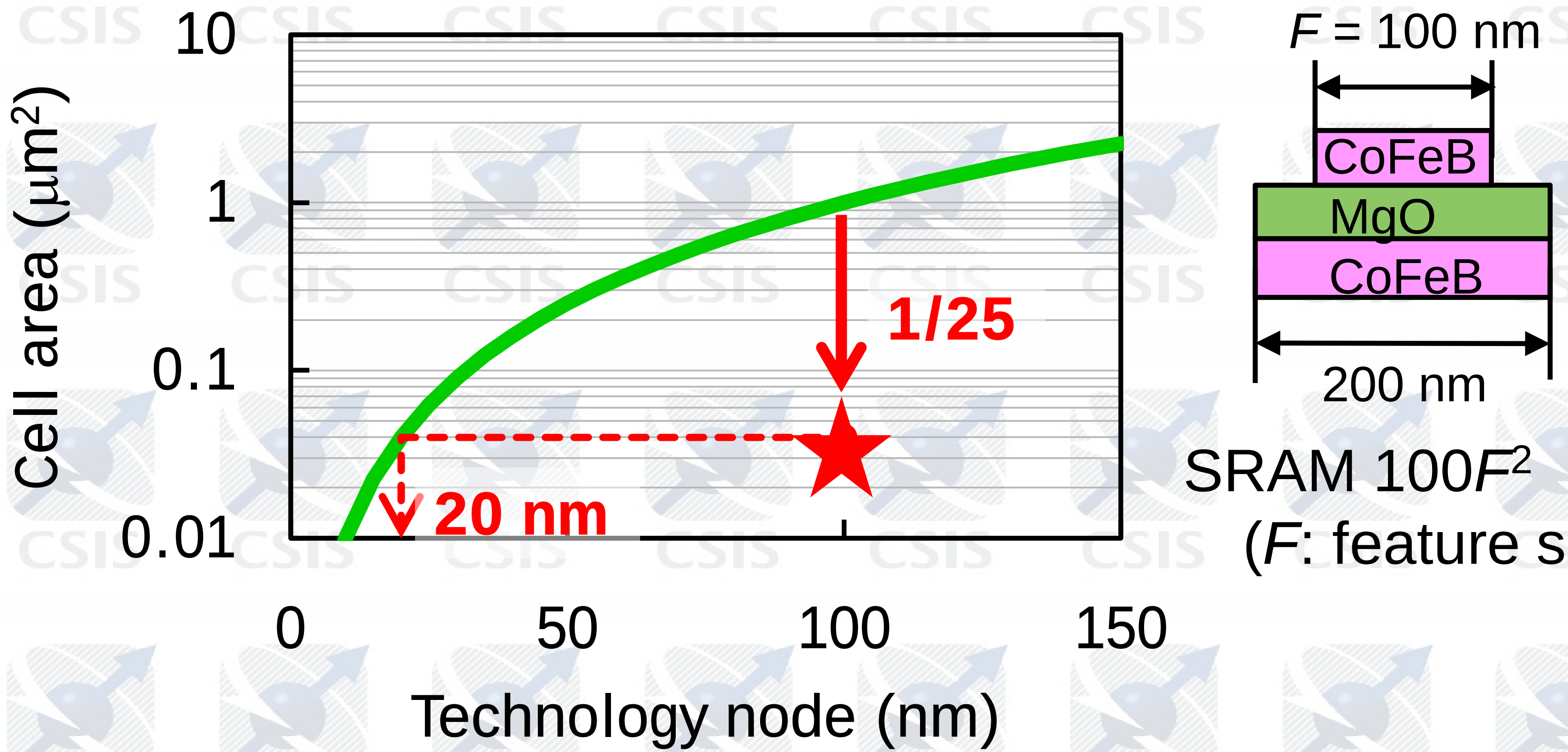
Cell area of stepped structure

- Cell area of stepped structure we demonstrated is 0.09 μm^2 which corresponds to SRAM cell area at 32 nm technology node.



Cell area of stepped structure

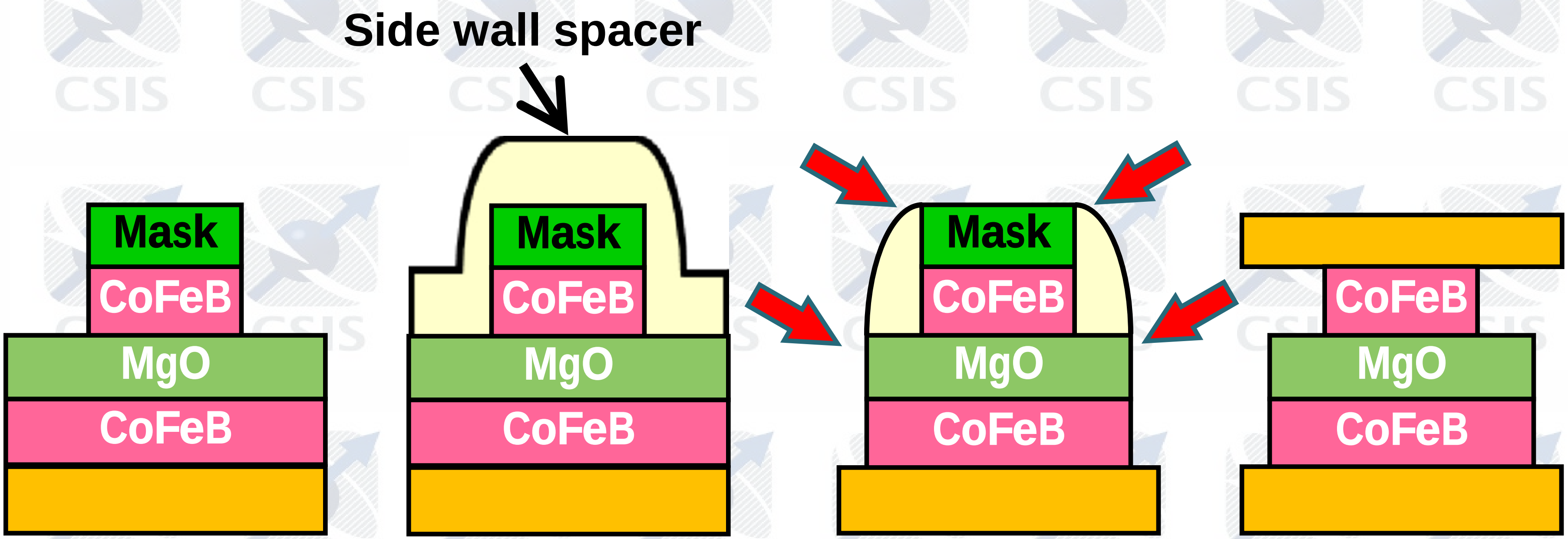
- Cell area can be down to 0.04 μm^2 without degrading the retention time over 10 years, which corresponds to SRAM cell area at 20 nm technology node.



SRAM 100F^2
(F: feature size)

For reducing fabrication cost

- Additional masks are not necessary



1. Fabrication the free layer
2. Deposition of side wall spacer
3. Etchback
4. Completion of stepped structure

Summary

- Novel MTJ structure “stepped structure” is proposed.
- Different retention times of “0” and “1” information are symmetrized.
- The stepped structure achieves retention time over 10 years.
- The cell area of the stepped structure corresponds to that of SRAM at 20 nm technology node.
- Self-alignment process for reducing fabrication cost is also proposed.