MTJ-Based Nonvolatile Logic-in-Memory Architecture

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Outline

• Nonvolatile Logic-in-Memory Architecture Overview

• NV GP-Logic: Nonvolatile-FPGA

• NV SP-Logic: Nonvolatile-TCAM

• Conclusions & Future Prospects
Background: Increasing delay & power

- Logic and Memory modules are separated
- Many interconnections between modules
- Wire delay dominates chip performance
- Global wires require large drivers.

On-chip memory modules are volatile.

- Power supply must be continuously applied in memory modules.

Delay: Long  Power: Large

Static power: Large
Nonvolatile logic-in-memory architecture

- Logic-in-Memory Architecture (proposed in 1969):
  Storage elements are distributed over a logic-circuit plane.

- MTJ device
- CMOS layer
- MTJ layer

- No volatility
- Unlimited endurance
- Fast writability
- Scalability
- CMOS compatibility
- 3-D stack capability

- Storage is nonvolatile:
  (Leakage current is cut off)
  Static power is cut off.
  Chip area is reduced.
  Wire delay is reduced.
  Dynamic power is reduced.

- MTJ devices are put on the CMOS layer

- Storage/logic are merged:
  (global-wire count is reduced)
Implementation of MTJ Device

MTJ Device stacked over MOS Plane

The area cost using MTJ device is small.

D. Suzuki, et al., VLSI Circuit Symp. 2009
Power-gating suitability

- **Power switch**
- **Leakage current**
- **Power switch**

**External Nonvolatile storage**

**Power switch**

**Volatile storage**

**Logic**

**Power switch**

**VDD**

- **Active**
- **Standby**
- **Active**

**Power switch (PMOS)**

**Nonvolatile storage (MTJ device)**

**Logic**

NV logic-in-memory architecture

Power gating is performed without data backup/reload.
Nonvolatile Processor Architecture

1st-step Nonvolatile Processor

2nd-step Nonvolatile Processor

GP-Logic: General-purpose logic
SP-Logic: Special-purpose logic

Nonvolatile Field-Programmable Gate Array (FPGA)
Nonvolatile Ternary Content-Addressable Memory (TCAM)
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Nonvolatile Field-Programmable Gate Array (FPGA)

-- Arbitrary logic functions are performed and programmed by FPGA
-- Power dissipation and hardware overhead are two major issues.
-- NV storage elements are distributed over the NV-FPGA (no external NVM).

😊 Leakage current elimination and short latency are possible.

😊 How to design?

Nonvolatile logic-in-memory architecture

Not required!
Conventional nonvolatile FPGA

😊 CMOS logic circuit requires high-voltage input swing.

How do we perform logic operation by using low swing signal from MTJ device directly?
MOS/MTJ-hybrid circuitry (Proposed)

Current-mode logic (CML)

😊 Logic operation is performed even low swing voltage by using the small difference of the current value.

Device count is reduced to 28% with less performance degradation.
Logic operation in low swing voltage is performed by using a MOS/MTJ-hybrid network.
### Test chip features

<table>
<thead>
<tr>
<th>Process</th>
<th>0.14µm MTJ/MOS 1-Poly, 3-Metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>287µm²</td>
</tr>
<tr>
<td>MTJ Size</td>
<td>50nm × 150nm</td>
</tr>
<tr>
<td>TMR Ratio</td>
<td>100%</td>
</tr>
<tr>
<td>Write</td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>150µA</td>
</tr>
<tr>
<td>Time</td>
<td>10ns</td>
</tr>
</tbody>
</table>

**Standby Current**: 0A

**Fabricated 2-input LUT**

4 MTJ devices are stacked over MOS layer

Measured waveforms (Basic operations)

<table>
<thead>
<tr>
<th>Input A</th>
<th>Input B</th>
<th>Output Z</th>
<th>Output Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
<td>Z</td>
<td>Z</td>
</tr>
</tbody>
</table>

- **NOR**:
  - Input A: '1', '0', '0', '0', '1', '1', '1', '0'
  - Input B: '0', '1', '1', '0', '1', '0', '0', '1'
  - Output Z: '0', '1', '0', '0'

- **NAND**: (Waveform not shown)

- **XOR**: (Waveform not shown)

- **XNOR**: (Waveform not shown)

**Scales**:
- **Vertical**: 0.78V/div
- **Horizontal**: 100μs/div

**Timing**:
- **Pre-Charge (P)**: 100μs/div
- **Evaluate (E)**: 100μs/div
Immediate wakeup behavior has also been measured successfully.
## Comparison of performances

<table>
<thead>
<tr>
<th></th>
<th>Nonvolatile SRAM *1)</th>
<th>Proposed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Counts</td>
<td>102 MOSs + 8 MTJs</td>
<td>29 MOSs + 4 MTJs</td>
</tr>
<tr>
<td>Area *2)</td>
<td>702 µm²</td>
<td>287 µm²</td>
</tr>
<tr>
<td>Active</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Delay *3)</td>
<td>140 ps</td>
<td>185 ps</td>
</tr>
<tr>
<td>Power *3)</td>
<td>26.7 µW</td>
<td>17.5 µW</td>
</tr>
<tr>
<td>Standby</td>
<td>Power</td>
<td>0 µW</td>
</tr>
</tbody>
</table>

*2) Estimation based on a 0.14µm process
*3) HSPICE simulation based on a 0.14µm MOS/MTJ-hybrid process
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Ternary Content-Addressable Memory (TCAM)

Fully parallel search and fully parallel comparison can be done. TCAM is a “functional memory.” TCAM is the powerful data-search engine useful for various applications such as database machine and virus checker in network router.

TCAM must be implemented more **compactly** with **lower power** dissipation.
## NV-TCAM Cell Function

<table>
<thead>
<tr>
<th>Stored data</th>
<th>Search input</th>
<th>Current comparison</th>
<th>Match result</th>
</tr>
</thead>
<tbody>
<tr>
<td>B $(b_1, b_2)$</td>
<td>$S$</td>
<td>$I_Z &lt; I_Z'$</td>
<td>ML</td>
</tr>
<tr>
<td>0 $(0,1)$</td>
<td>0</td>
<td>$I_Z &gt; I_Z'$</td>
<td>0 \ (Mismatch)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>$I_Z &gt; I_Z'$</td>
<td>0 \ (Mismatch)</td>
</tr>
<tr>
<td>1 $(1,0)$</td>
<td>0</td>
<td>$I_Z &gt; I_Z'$</td>
<td>0 \ (Mismatch)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>$I_Z &lt; I_Z'$</td>
<td>1 \ (Match)</td>
</tr>
<tr>
<td>X \ (don’t care)</td>
<td>$0,0$</td>
<td>$I_Z &lt; I_Z'$</td>
<td>1 \ (Match)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>$I_Z &lt; I_Z'$</td>
<td>1 \ (Match)</td>
</tr>
</tbody>
</table>
CMOS-based TCAM cell circuit

- Transistor counts: **12** (ED; 4T, 2-bit storage; 8T)
- Input/output wires: **8** (BL; 2, WL; 1, $V_{DD}$&$V_{SS}$; 2, SL; 2, ML; 1)
- Always supply the power: **Many leakage current path**

How to realize compact & cut off the leakage current?
MOS/MTJ-hybrid TCAM cell circuit

- Merge storage into logic circuit: Compact (2T-2MTJ)
- Share wires: 4 (ML/BL, SL/WL, No-V_{DD})
- 3-D stack structure: Great reduction of circuit area

Compact & nonvolatile TCAM cell with MTJ devices

Power-Gating Scheme of Bit-Serial NV-TCAM

According to the word length of the TCAM, the effectiveness of the standby-power reduction is increased.

TCAM cell circuit test chip

Chip features

<table>
<thead>
<tr>
<th>Process</th>
<th>0.14µm CMOS/MTJ 1-Poly, 3-Metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total area</td>
<td>29.4 µm²</td>
</tr>
<tr>
<td>TCAM cell size</td>
<td>3.15 µm² (2.1 µm × 1.5 µm) a)</td>
</tr>
<tr>
<td>Cell structure</td>
<td>2MOSs-2MTJs</td>
</tr>
<tr>
<td>MTJ size</td>
<td>50 nm × 200 nm</td>
</tr>
<tr>
<td>TMR ratio</td>
<td>167%</td>
</tr>
<tr>
<td>Average write current</td>
<td>274 μA (τₚ = 10 µs) b)</td>
</tr>
<tr>
<td>Standby current</td>
<td>0A (Power off)</td>
</tr>
</tbody>
</table>

a) A CMOS-based TCAM cell with 12 transistors, whose cell size is 17.54 µm² under a 0.18 µm CMOS process, has been reported.8) The size of the conventional TCAM cell can be estimated as 10.61 µm² under a 0.14 µm CMOS process by scaling down. Thus, the size of the fabricated TCAM cell is reduced to 30 % compared to that of the conventional one. Moreover, minimum size of the proposed TCAM cell can be considered as 1/6 of the conventional one.

b) More high-speed write operation is possible with increase of write current. For example, with the average current of 327 µA at 10 ns write.
Waveforms of equality-search operations

P : Precharge phase  E : Evaluate phase

 CLK

S

Search data

OUT

Match result

Stored data B=1

S=0  S=1

Match

Mismatch

Match

Mismatch

Match

Mismatch

Match

Stored data B=0

S=0  S=1

Match

Mismatch

Match

Mismatch

Match

Stored data B=X

S=0  S=1

Match

Mismatch

Match

Mismatch

Match

Bit-level equality-search is successfully demonstrated.
Waveforms of sleep/wake-up operations

Instant sleep/wake-up behavior is successfully demonstrated.
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Conclusions

Propose a MOS/MTJ-hybrid circuit (nonvolatile logic-in-memory circuit using MTJ devices) style
Two kinds of typical applications with logic-in-memory architecture; NV-LUT circuit and NV-TCAM
Compact and no static power dissipation
Confirm basic behavior with fabricated test chips under an MTJ/CMOS process.
It could open an ultra-low-power logic-circuit paradigm

Future Prospects and Issues:
1. Establish the fabrication line
2. Establish the CAD tools
3. Explore the appropriate application fields (Impact towards “Reliability Enhancement”)