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Tohoku University

Spintronics research center has demonstrated a series of ultra-low power spintronics-based large-scale integrated circuits

－Summary of main research achievements of the FIRST Program "Research and development of ultra-low power spintronics-based VLSIs"－

[Abstract] Center for Spintronics[1] Integrated Systems (CSIS) led by Professor Hideo Ohno, Director of CSIS and Professor of the Research Institute of Electrical Communication (RIEC), Tohoku University, together with joint project organizations, has been conducting the "Research and Development of Ultra-low Power Spintronics-based Very Large Scale Integrated Circuits (VLSIs)" project: supported by Japan Society for the Promotion of Science's FIRST program from FY 2009 through FY 2013. Through the FIRST funding, CSIS has successfully established and demonstrated (1) a technology development structure that encompasses spintronics materials, devices, processes, and circuit design in a 300 mm fabrication platform for spintronics-based VLSIs, (2) prototypes of spintronics-based logic integrated circuits composed of millions of transistors and high performance perpendicular easy-axis magnetic tunnel junctions (MTJs) developed at CSIS, and (3) superior performance (chip area ratio × delay time ratio × power consumption ratio ≤ 1/64) of these circuits compared with conventional CMOS technology. These achievements show that CSIS is the world's first and so far only spintronics research center in which the coherent research and development of spintronics materials, devices, integration processing, and circuit design are being carried out. Based on the established development and fabrication platform, CSIS will continue to demonstrate spintronics-based logic integrated circuits aiming at practical use.

[Background]

Logic integrated circuits, where intelligent systems are integrated on a single chip die, form the key technology in modern society, determining the quality of a vast array of systems as well as the social infrastructure. Looking back at the history of integrated circuits, ground-breaking innovation that forces paradigm shift occurred when the power consumption of logic LSIs reached its limit due to increasing density and speed. Currently, both standby/operating power consumption in logic VLSIs are poised to reach their upper limits, and innovative new breakthroughs for low power technology are thus required. In order to overcome the power consumption limitation, a paradessential expedient to 1) reduce operating power consumption, 2) achieve no or ultra-low standby power consumption, and 3) increase performance needs to be stated. One method of doing this is embedding high performance non-volatile devices, in which stored information can be retained even in power off condition, into logic integrated circuits. Spintronics devices composed of magnetic tunnel junctions are the only candidate for applying non-volatile logic LSIs due to their non-volatility, high speed, low voltage, non-destructive read operation, virtually infinite read/write endurance, device scaling capability, and compatibility with conventional VLSI manufacturing processes. Therefore, to push forward innovative breakthroughs in future logic integrated circuits, we need to develop a high performance spintronics device and use it to design and fabricate a spintronics-based VLSI and show its promised high potential.

[Research program]

With the "Research and Development of Ultra-low Power Spintronics-based VLSIs" project (core researcher: Hideo Ohno), which started in March 2010 and is financially supported by a grant from the Japan Society for the Promotion of Science (JSPS) through "Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program)," initiated by the

Council for Science and Technology Policy (CSTP), CSIS aims to assume a leading role in achieving paradigm change in VLSIs by developing high performance spintronics[1] devices and by embedding these devices into logic integrated circuits. In this way, the center plays a pivotal role in the world-wide innovation cycle of logic VLSIs.

[Main research achievements]

1) Development of high performance spintronics device; magnetic tunnel junctions (MTJs)[2]

We developed perpendicular easy-axis MTJs composed of double CoFeB-MgO[3] interfaces with high performance, high reliability, and low switching power consumption. These MTJs have the following properties at a junction diameter of 20 nm: 1) the world's highest thermal stability[4] of $\Delta = 58$, 2) a high tunnel magnetoresistance ratio[5] of 100%, and 3) a low switching current of 24 μA. Moreover, we fabricated the world's smallest MTJ at a junction diameter of 11 nm and demonstrated the fundamental performance of tunnel magnetoresistance effect and current induced switching. This was the world's first demonstration of a spintronics device for 20-nm LSI generation or less, where conventionally it has been difficult to manufacture memory devices.

2) Design, fabrication, and demonstration of spintronics-based VLSIs

In order to demonstrate high performance of spintronics-based VLSIs particularly with ultra-low power consumption, we designed, fabricated, and evaluated spintronics-based VLSIs composed of millions of transistors and perpendicular easy-axis MTJs developed at CSIS on a 300-mm silicon wafer using 90-nm CMOS technology. These VLSIs included i) a high speed spintronics memory embedded in high performance logic integrated circuits as a cash memory, ii) a non-volatile field-programmable gate array (FPGA) to be configured by the customer after manufacturing, iii) a non-volatile ternary content-addressable memory (TCAM) for a high-speed fully-parallel data search system, and iv) a non-volatile microcontroller (MCU) for wireless sensors networks. These spintronics-based VLSIs with non-volatile, high performance features showed nearly two orders of magnitude superior performance (chip area ratio × delay time ratio × power consumption ratio ≤ 1/64) compared with conventional CMOS technology without MTJs.

3) Establishment of a platform for design, fabrication, and demonstration of spintronics-based VLSIs

CSIS has established the technology structure of spintronics-based logic integrated circuits and established a design and fabrication platform at Tohoku University. CSIS has started promoting world wide collaboration by inviting researchers from Japan and overseas to CSIS to expand and enhance spintronics technology research and development activities. While the FIRST program will be completed as planned by March 31, 2014, CSIS will continue to proceed by further demonstration of spintronics-based VLSIs aiming at practical use. Particularly, CSIS continues to assume a leading role in the innovative changes in VLSIs brought about by spintronics technology in collaboration with the Center for Innovative Integrated Electronics Systems (CIES; Director: Prof. Tetsuo Endoh) at Tohoku University based on various programs and the cooperation among government, industry, and academia.

CSIS Research Review will be held on March 14, 2014 at the Tokyo International Forum, Hall D7.
Web site: http://www.csis.tohoku.ac.jp/files/20140314_day2_e.pdf

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Notes:

1. Spintronics

Spintronics, also known as magnetoelectronics, is an emerging technology that exploits two features of the electron, its intrinsic spin and its associated magnetic moment, in addition to its fundamental electronic charge, in solid-state devices, such as magnetic devices and electron devices. Concentrated efforts have been made to develop electronics equipment using both higher density data storage magnetic devices (hard disks) and higher speed electron devices (semiconductor integrated circuits) independently. Spintronics is expected to emerge as a breakthrough technology for future ultra low power and high speed integrated circuits, leading to zero standby power electronics equipment.

2. Magnetic tunnel junctions (MTJs)

Magnetic tunnel junctions consist of a structure in which two ferromagnetic electrodes sandwich an insulating layer. When the magnetization direction between the two electrodes is parallel (antiparallel), the resistance shows a low (high) value, which is called the tunnel magnetoresistance effect.

3. CoFeB-MgO

CoFeB-MgO is the material used in the system that demonstrated the world's highest tunnel magnetoresistance ratio at room temperature by a research group at Tohoku University in 2008. This same research group first fabricated CoFeB-MgO magnetic tunnel junctions with a perpendicular easy-axis by making use of special magnetic anisotropy at the CoFeB-MgO interface and demonstrated the strong performance of CoFeB-MgO magnetic tunnel junctions at the junction diameter of 40 nm. The group then developed a structure using double CoFeB-MgO interfaces and was able to increase the thermal stability factor without increasing the writing current.

4. Thermal stability

Thermal stability is a factor determining retention time. Δ can be expressed by the energy barrier E that separates two magnetization configurations divided by thermal energy k_BT, $\Delta = E/k_BT$.

5. Tunnel magnetoresistance ratio

Tunnel magnetoresistance ratio is a factor in the evaluation of the tunnel magnetoresistance effect. Tunnel magnetoresistance ratio can be expressed by using resistance at parallel configuration (R_P) and at antiparallel configuration (R_{AP}), as $(R_{AP}-R_P)/R_P$.