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Demonstration of 20-nm magnetic domain wall motion memory

Tohoku University confirmed excellent scalability and high-speed and low-power-operation capability

[Abstract] The research group of Professor Hideo Ohno of Center for Spintronics Integrated Systems, Research Institute of Electrical Communication, and WPI Advanced Institute for Materials Research of Tohoku University together with the group of Professor Teruo Ono of Institute for Chemical Research of Kyoto University fabricated and evaluated magnetic domain wall motion memory devices, which is expected to be applied to spintronics-based very large-scale integrated circuits (VLSIs), and found that this device has an excellent scalability and high-speed and low-power-operation capability. They successfully demonstrated a good operation of the world's smallest domain wall motion device with the width of 20 nm and revealed that it is possible to program to this device with the world's smallest electric power, which is more than one order of magnitude smaller than the state-of-the-art value obtained in a spintronics device. The obtained results indicate that the domain wall motion device is applicable to the leading-edge and future semiconductor technologies and the spintronics-based VLSIs with this device can be utilized to a wide variety of applications.

[Background and research issue]

"Size reduction enhances the performance" – thanks to this feature, the semiconductor-based very large-scale integrated circuits (VLSIs) have made great progress for several decades. However, now it faces a new stage, where "the size reduction cannot enhance the performance furthermore (*1)" or "the size reduction itself is difficult (*2)." These issues are mainly owing to the principle of semiconductor-based VLSIs, which are based on the *electric charge* of the electron. This is why the spintronics-based VLSIs now attract a great deal of attentions. In the spintronics VLSIs where nonvolatile spintronics devices (*3) are embedded into the conventional semiconductor-based VLSIs, the fully-established excellent features of the semiconductor technology is utilized as in the past and storage units in which standby power and stable operation have become serious issues are replaced by the spintronics devices, which utilize both *electric charge* and *spin* of the electron. Then one can continue the scheme that "size reduction enhances the performance" and, at the same time, drastically reduce the standby power because the spintronics devices need no electric power to retain the information.

A three-terminal magnetic domain wall motion memory device (*4), one of the spintronics devices, has been expected to be applied to the cache memories and temporary storage circuits composed by such as SRAMs (*5) in the currently-used semiconductor-based VLSIs. Up to now, basic operation and high reliability have been confirmed in the domain wall motion device with the width of around 100 nm.

Size reduction of the circuit pattern in the semiconductor VLSIs has been advancing year by year and the leading edge size of the research and development is around 32 – 16 nm. In order to apply the spintronics devices to the leading edge and future semiconductor technologies, the spintronics devices should be able to reduce their size down to such dimensions with maintaining the good properties; this feature is called as "scalability." However, studies addressing such issues have not been fully carried out to date.

[Technical method and achievement]

The group consisting of Tohoku University and Kyoto University fabricated the domain wall motion devices with various

wire widths down to 20 nm and evaluated their domain wall motion properties, retention properties, and size dependence of these properties. They demonstrated a good operation in 20-nm-wide device which is far narrower than the previously-reported devices. Also, from the evaluation on the size dependence of device properties, they revealed the excellent scalability of this device as follows:

1) The current required to program decreases linearly with the device size.
2) The time required to program also decreases linearly with the device size.
3) The sufficient retention property, i.e., thermal stability, can be maintained regardless of the device size.
4) The write error rate can be also suppressed to extremely low level regardless of the device size.

In addition, they estimated the power required to program to one bit of the domain wall motion device to be 1.8 fJ at the device width of 20 nm. This value is 1/50 of the state-of-the-art reported in a work on another type of spintronics device previously (90 fJ) and almost as small as the one for one bit of SRAM. This indicates that the domain wall motion device is very promising in terms of not only the standby power, but also the dynamic power.

[Significance of research]

The present research has two significances. The first one is that the domain wall motion device is found to be applicable to the leading edge and future generation semiconductor VLSIs. Thus, the spintronics VLSIs with the domain wall motion device allow one to reap the benefit of semiconductor VLSIs that "size reduction enhances the performance" continuously. The second one is that the power consumption for the data programming in the domain wall motion device at reduced dimensions is found to be as small as the one in the semiconductor VLSIs. This indicates that the spintronics VLSIs with the domain wall motion device can be utilized to a wide variety of applications.

Tohoku University and Kyoto University announced their latest results on December 9 at the 2013 IEEE International Electron Devices Meeting (December 9-11, Washington, D.C., USA).

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Notes:

(*1) The leakage current in the metal-oxide-semiconductor field-effect transistor (MOSFET), which is the most important building block of the semiconductor-based VLSIs, has been increasing, and, as a result, the increase in power dissipation during standby mode has been aggravated. Also, since the memory blocks and logic blocks are located separately with connected by

global wiring in the currently-used VLSIs, power dissipation during the data transmission and data transfer delay has become a bottleneck for the performance as the amount of information increases due to the high integration.

(*2) DRAMs (*5), which are usually used in a main memory of integrated circuits, store the information as electric charge in a capacitor. The capacitor should have sufficient capacitance for the stable operation. The capacitor is formed by digging a trench. The decrease in the capacitance due to the size reduction was overcome by deepening the trench to date, but a technical limit of fabrication is approaching recently. Also, in SRAMs, it becomes difficult to secure the circuit operation margin due to the increase in the intrinsic variability of threshold voltage of MOSFET as the device size is reduced.

(*3) Whereas, in SRAMs and DRAMs, source voltage should be supplied for the retention of information even in the standby mode; this property is called as volatility, in the spintronics devices, the information can be retained even though the source power was turned off; this property is called as nonvolatility. Therefore, replacing the volatile memories by nonvolatile memories allows one to drastically reduce the power consumption during the standby mode.

(*4) Magnetic domain is a region in which magnetic moments are aligned in ferromagnetic materials, and magnetic domain wall is the boundary region between the magnetic domains. It is known that the domain wall is moved in the direction of electron flow through the effect of angular momentum conservation and quantum mechanics when the current passes through the domain wall; this phenomenon is called current-induced domain wall motion. In the three-terminal magnetic domain wall motion device, the magnetization reversal due to the current-induced domain wall motion is utilized for the writing method and tunnel magnetoresistance effect is used for the reading method. The three-terminal domain wall motion device achieves high-speed and reliable operation due to a large operation margin because the read and write current paths are different each other.

(*5) SRAM: Static Random Access Memory, DRAM: Dynamic Random Access Memory