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Tohoku University Develops
World's First Nonvolatile Memory Applicable to L3 Cache

A group led by Professor Hideo Ohno, of the Center for Spintronics Integrated Systems and of the Research Institute of Electrical Communication, Tohoku University, Sendai, Japan, and by Professor Tetsuo Endoh, of the Center for Spintronics Integrated Systems and of the Graduate School of Engineering, Tohoku University, has developed the world's first embedded memory that can transfer data as fast as today's state-of-the-art static random access memory (SRAM)[1] and that can retain data even without power. They did this by combining the magnetic tunnel junction (MTJ) technology extensively researched and developed at Tohoku University with state-of-the-art silicon technologies in an academic-industrial alliance with NEC Corporation, Tokyo, Japan. The operating principle of the memory was verified by measuring the performance of a 1-Mb nonvolatile embedded memory macro fabricated in the Tsukuba Innovation Arena (TIA)[2], Tsukuba, Japan, and based on the MTJ fabrication technology developed at Tohoku University. This achievement is a major step toward lowering the power consumption of today's computing systems, which is important given that the performance gains being made by miniaturization of the constituent LSI chips come at the cost of an increase in power consumption.

The MTJ technology developed at Tohoku University is a spintronics technology in which the interaction between an electron's electrical charge and its quantum mechanical properties (i.e., 'spin') plays a crucial role in controlling the material's electrical features. An MTJ has two thin magnetic layers separated by a thinner dielectric film. The electrical current flowing through this sandwich structure changes depending on the relative direction of the spins in the two magnetic. Switching between a higher resistance state and a lower resistance one is done by applying voltage between the two magnetic layers in different directions. The states maintain their characteristics even after the voltage is removed (nonvolatile feature), with virtually unlimited switching potential. The use of MTJs makes it possible for the memories, latches, and flip-flops[3] used in logic LSI devices to be powered down without any loss of their stored data. The MTJs are key devices for use in the logic and working memories of the

computer components of future super-low-power electrical appliances.

The members of the Endoh Laboratory at Tohoku University are investigating a new memory hierarchy[4] for use in future high-performance and low-power computing systems. The bottleneck in improving the performance of today's computers is two-fold: (1) the speed gap between the main memories and data storage memories is increasing, and (2) the power consumption of the working memories (SRAM's cache memories and DRAM's main memories) is increasing due to leakage from the off-state transistors and capacitors. Their goal is to implement nonvolatile memories using MTJs and CMOS circuits into a computer's memory hierarchy. The introduction of nonvolatile memories that have much faster data transfer than today's data storage memories is expected to eliminate the speed gap. Their introduction is also expected to reduce the power consumption of state-of-the-art working memories by shutting down the power supply when they are not accessed.

However, a large current is needed to switch an MTJ as quickly as required by the computer's working memories. Moreover, the probability of successful switching is reduced if the MTJ is to be switched too quickly. Therefore, the ability to write data to MTJ-based nonvolatile memory within a few nanoseconds, as required for the working memories, has not yet been achieved.

The members of the Endoh Laboratory have developed a circuit technology that uses a background write scheme to get around this problem. The scheme was implemented in 1-Mb nonvolatile embedded memory, and a 2.1-ns write cycle was demonstrated. This is the world's fastest write cycle and is applicable to L3 cache memory. The scheme is based on a memory cell consisting of a conventional SRAM cell and a pair of MTJs that are connected to the data storage nodes in the SRAM. It features a newly developed switching concept: the two MTJs are switched autonomously by using data that was written in a short time span into the SRAM even if the write cycle terminated before the MTJs were switched. Since this operation is autonomously performed in a memory cell or without an external write operation, the next read or write operation can be cycled without interrupting it. The memory's write cycle time is thus limited only by the SRAM's write time, making the memory's write very fast with nonvolatile features. The cell's power supply can be terminated after the MTJ switching has ended, thereby eliminating the need for standby power.

The developed 1-Mbit nonvolatile embedded memory macro, which was fabricated using 90-nm CMOS and 100-nm MTJ technologies, provides the high-speed data-read and -write cycles required by L3 cache memory and enables data to be retained without power. This technology can be used to make today's cache memories nonvolatile, solving the problem of power consumption by computers.

These new developed technologies have several key features:

i) Autonomous switching of MTJs in MTJ/CMOS hybrid memory cell

This is the first scheme proposed for autonomous switching in a memory cell consisting of an SRAM cell and a pair of MTJs. This scheme switches the MTJs, which require a relatively long period for switching, by using data in the SRAM, which has a shorter switching period, even if the write cycle has finished. Since this switching is performed autonomously in individual cells, secure and stable MTJ switching can be performed at a delay following the fast read and write operations required for L3 cache.

ii) Fast nonvolatile working memories applicable to cache

A 1-Mb nonvolatile embedded memory macro was designed with this autonomous switching mechanism and fabricated using 90-nm CMOS and 100-nm MTJ technologies. It can perform random reads in 1.5 ns and random writes in 2.1 ns. This is the fastest cycle reported for nonvolatile memory using MTJs.

Tohoku University and NEC are developing nonvolatile logic LSI devices using MTJs as part of its efforts to develop super-low-power computers. Combined with the development of nonvolatile logic LSI devices, the achievement of this nonvolatile embedded memory macro marks a step forward in achieving super-low-power computers. That is, it will lead to LSI devices that are standby-power-free without interfering with the trend toward higher performance.

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(notes)

1. SRAM

SRAM stands for static random access memory, which is commonly embedded in logic LSI devices. Data is stored in a circuit with six transistors, and the access time is short enough for the access to be synchronized with the logic data processing. The data is lost if the memory is powered down (i.e., the data is volatile).

2. Tsukuba Innovation Arena (TIA)

This hub for nano-technology research was established in 2009 by the National Institute of Advanced Industrial Science and Technology (AIST), National Institute for Materials Science (NIMS), and the University of Tsukuba to integrate their research capabilities and to formulate a global center for nano-technology innovation in Tsukuba, Japan.

3. Latches and flip-flops

A latch is a device for storing one-bit data in synchronization with a signal. A flip-flop is formed by combining two latches to create a circuit for storing data. They are commonly used in today's mainstream LSI data processing.

4. Memory hierarchy

Computers typically consist of a core processor, cache memories (L1, L2, and L3), main memory, and data storage memory. These memories constitute a memory hierarchy in which cache is the fastest and has the smallest capacity while the data storage is the slowest and has the largest capacity. The main memory sits in between. The three cache levels (L1, L2, and L3) have increasingly faster access in that order. The cache and the main memory are made of SRAM and DRAM, respectively, where DRAM is the smallest memory device that stores data in a capacitor switched by a transistor and must be regularly refreshed to prevent data loss due to leakage.

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