東北大学

Empowered by Innovation

NEC

February 19, 2013

Tohoku University
NEC Corporation

Automatic design flow of nonvolatile logic-in-memory integrated circuits with spintronics devices established

Demonstration of image-processing with reduced power consumption

Tohoku University and NEC Corporation have adopted spintronics technology in logic integrated circuits to achieve “zero standby power” in electronic devices. Moreover, they have developed a library that establishes automatic design flow of nonvolatile logic-in-memory integrated circuits, where nonvolatile storage elements are distributed over a logic-circuit plane. Using this library, they have successfully designed and fabricated a prototype image processing chip and demonstrated that it reduces unnecessary power consumption by up to 75%.

This technology is one of the spintronics-based logic integrated-circuit technologies that capitalize on the spin[*1] of fine magnets and negative charges of electrons. By utilizing magnetic tunnel junction (MTJ) [*2] devices, which have long been under development by Tohoku University, all circuits on the logic integrated circuit can be made non-volatile.

Tohoku University and NEC have demonstrated the functionality of circuits and circuit components with a small number of regularly lined MTJ devices, such as general-purpose data-search hardware (TCAM), logical operation circuits for FPGA (LUT), etc[*3]. However, large-scale logic integrated circuits usually have a large number of MTJ devices that

are arranged in a complex and irregular manner, requiring the use of automatic design tools that can be applied to a nonvolatile logic-in-memory circuit.

This newly developed library will be used in addition to existing logic-circuit design tools that use computer aided design (CAD) and will enable the design of large-scale logic-in memory integrated circuits, even without expertise in circuit design or spintronics technology.

Nonvolatile logic-in memory integrated circuits enable the power to be turned off in circuits not needed for carrying out logical operations. This allows the development of devices with zero standby power, energy-efficient operations and instantaneous start-up. Automatic design tools equipped with this newly developed library were used to test-manufacture and demonstrate the functionality of a processor for image processing. As a result, it was found that processors using the newly developed library required zero standby power and enabled the reduction of power consumption that is not necessary for operation to 1/4 that of processors that do not use spintronics technology.

Key features of the technology are as follows.

1. Development of an automatic design library that supports irregular and complex non-volatile logic-in memory integrated circuits

A library that can be incorporated in automatic design tools was created for designing nonvolatile logic-in-memory integrated circuits with irregular and complex circuit architecture. This library enables logic synthesis and automatic layout similar to those in common

integrated circuits while utilizing non-volatile MTJ devices for the memory.

2. Use of the design tool to develop an image processor that reduces unnecessary power consumption during operations by 75%

Nonvolatile logic-in-memory integrated circuits enable the reduction of wasteful power consumption by turning off the power for circuits not needed during logic operations. By running only the needed processors out of the 25 processors for each operation and turning off the power for the unused ones, the newly developed image processor reduces unnecessary power consumption to 1/4 that of processors not utilizing the technology.

Together with the expansion of cloud computing, the use of information and communication equipment has remarkably increased in recent years. Current devices, however, usually require a considerable amount of time for starting up once their power is completely turned off, and internal circuits are usually kept powered on during standby to maintain data. Thus, there is a growing concern about the increase in needed standby power arising from the increase in the number of devices.

Tohoku University and NEC Corporation are working together to further improve the spintronics logic integrated circuit technology in order to develop larger-scale and more power-efficient integrated circuits for a wide range of uses as well as to pursue the early commercial development of the technology.

Tohoku University and NEC will announce the above results during

the International Solid-State Circuits Conference (ISSCC) 2013 to be held in San Francisco, California from February 17 to 21.

A portion of these results were produced through “Research and development into Energy Efficient Spintronics Logic Integrated Circuits”[*4] (headed by Prof. Hideo Ohno at Tohoku University), an advanced research and development program funded by the Cabinet Office.

***

Notes:

*1 "Spin" is one of the properties of electrons (an elementary particle with negative electric charge) that makes them behave like tiny magnets.

*2: A device that optimizes the architecture and materials of circuits to change the magnetization direction of fine magnets vertically.

*3: A joint initiative of Tohoku University and NEC Corporation
June 13, 2012 Press Release:
Groundbreaking New Technology for Improving the Reliability of Spintronics Logic Integrated Circuits: Progress towards the commercialization of circuits that enable electronic devices to consume zero standby power
http://www.nec.com/en/press/201206/global_20120611_02.html

*4: This is a national project aiming to improve Japan's competitiveness at the world level by concentrating on leading researchers of the most advanced technologies.

For inquiries contact:

Tohoku University:
Center for Spintronics Integrated Systems
Deputy Director Naoki Kasai
+81-22-217-6115
E-Mail：n-kasai@csis.tohoku.ac.jp
URL：http://www.csis.tohoku.ac.jp/

NEC:

For general public:

NEC Intellectual Assets R&D Unit Planning Division Public Relations Group
https://form.nec.jp/nec/276rd/4b126d/Inquiry.do?fid=4b126d

For press:

Ryoichi Yamanashi

NEC Corporate Communication Division

+81-3-3798-6511

E-Mail：r-yamanashi@ct.jp.nec.com