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Tohoku University

Tohoku University Develops the World's First 3-D Reconfigurable Spin Logic Chip with Spintronics Technology

Tokyo, June 4, 2012 – Tohoku University announces today that it has used spintronics technology to develop successfully the world's first 3-D stacked reconfigurable spin logic chip. The 3-D stacked reconfigurable spin logic chip is a key component of the ultra-high performance and ultra-low power reconfigurable spin processor that can vary a circuit's configuration in accordance with its uses and situations. The 3-D stacked reconfigurable spin logic chip can be achieved with 3-D LSI chip stacking and on-chip SPRAMs. From the SPRAM cell evaluation, the fastest write speed of 5 ns was obtained in the circuits. Moreover, parallel reconfiguration was fully demonstrated for the 3-D stacked reconfigurable spin logic chips for the first time. Both ultrafast on-chip SPRAM and 3-D stacked structure will replace conventional 2-D LSIs and open a new era of LSIs.

Recently, reconfigurable LSIs attract much attention as they can change circuit configuration accordingly with various uses and can achieve low cost and shorter developing time. Conventional reconfigurable LSIs consist of logic blocks, switch blocks, and SRAMs as working memory. Configuration data are supplied to SRAMs from external nonvolatile memory such as Flash memory, where the external nonvolatile memory works as a configuration memory. Therefore, such conventional reconfigurable LSIs require a longer configuration time due to long wiring between the working memory and configuration memory. To reconfigure quickly, both a shorter wiring length and a high-speed nonvolatile memory are indispensable. Moreover, parallel reconfiguration is also important to achieve high-performance reconfigurable LSIs with many cores. We have proposed a three-dimensional (3-D) stacked reconfigurable spin processor, where high-speed Spin-transfer torque RAM (SPRAM) is used as the configuration memory instead of the Flash memory. The 3-D stacked reconfigurable spin processor consists of several reconfigurable spin logic chips with on-chip SPRAMs and a multiple-core processor chip. These chips are stacked and connected with high-density Through-Si Vias (TSVs). In the 3-D stacked reconfigurable spin processor, configuration data are stored in the on-chip SPRAM. Therefore, circuit configuration becomes very fast. The parallel reconfiguration can be also performed due to 3-D stacked structure.

In this development, two reconfigurable spin logic chips were stacked and connected using 3-D integration technology including backside-via process. The fabrication procedure is as follows. First, the second layer chip was temporary bonded on a base wafer, and thinned and etched from the chip backside. Both Cu-TSV and Redistributed line (RDL) were simultaneously formed after SiO2 deposition with conventional electroplating. Then, many microbumps were formed on both first and second layer chips. Indium/Gold was used for low temperature bonding to avoid damages to magnetic tunnel junctions (MTJ) in SPRAM from high temperature process. The microbump height is 2 μm. After two chips were bonded and adhesives were injected, the base wafer was debonded. There are five metal layers beneath the In/Au microbump for the first layer chip, and Al/Ti RDL exists on In/Au microbump for the second layer chip. The SPRAM still has good spin-transfer torque switching behavior after the 3-D integration process. The second layer chip was thinned to 35 μm thick. Two chips were successfully stacked with 2232 TSVs and 2232 microbumps. Our 3-D integration process clearly does not affect MTJ behavior seriously. Finally, circuit functions of 3-D stacked reconfigurable spin logic chips were evaluated carefully. For parallel reconfiguration, single input LUT0~LUT3 was applied to the second layer chip (and the first layer chip through TSV), and then two outputs from the first and second layer chips were

recorded, like SIMD command. First, OUT signals were outputted in accordance with initial configuration saved in SRAM working memory. Then, SRAM data were rewritten with SPRAM configuration data, and OUT signals were outputted. Both OUT signals are clearly quite different between initial configuration and after reconfiguration. This means that high-speed parallel reconfiguration was completely performed in the 3-D stacked reconfigurable spin logic chips for the first time.

Key features of the 3-D stacked reconfigurable spin logic chip developments are as follows;
i. Low temperature 3-D integration technologies with backside-via process
High temperature process may degrade magnetic characteristics of magnetic tunnel junctions (MTJs) in SPRAM. Therefore, a low-temperature 3-D integration process was developed consisting of In/Au microbump bonding and electroplated Cu-TSV formation.

ii. Design of ultrahigh speed reconfiguration circuit in spin logic LSI
The reconfigurable spin logic LSI consists of a four-input Look-Up Table (LUT), an output flip-flop, and 16-bit SPRAM cells, and peripheral circuits. The four-input LUT consists of 16-input MUX and 16-bit SRAM. The 16-bit SPRAM is used for configuration memory, and SRAM is used for working memory. Ultra-high speed reconfiguration can be achieved by transferring data from SPRAMs to SRAMs or writing back data of SRAMs to SPRAMs.

We carefully designed a reconfigurable spin logic chip that has on-chip SPRAMs and successfully stacked these two spin logic chips using 3-D integration technology including backside-via process. From the SPRAM cell evaluation, the fastest write speed of 5 ns was achieved in the circuits. For the first time, parallel reconfiguration was perfectly demonstrated for the stacked reconfigurable spin logic chips. These results verified great significance of both ultra-fast on-chip SPRAMs and 3-D stacked structures.

Tohoku University will announce the latest results on June 14 at VLSI Symposium on Technology 2012 (June 11-15, Honolulu, Hawaii).

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