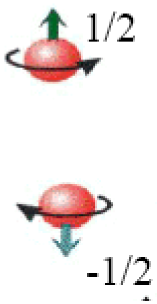
RECENT PROGRESS AND EMERGING TECHNOLOGIES OF SPINTRONICS DEVICE FOR VLSI

MAGNETISM BASICS

Electrons have a charge <u>and a spin</u>

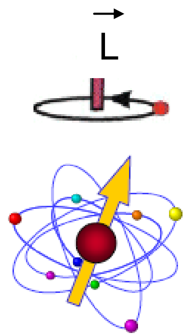
Spin moment



$\vec{S}$=+1/2 or -1/2

Orbital moment
+ Spin moment
+ Spin-Orbit

Atomic Moment

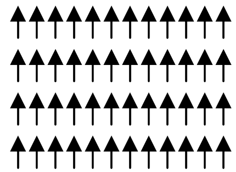


$\vec{J} = \vec{L} + \vec{S}$

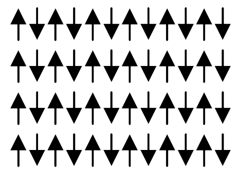
Exchange Interactions

$-J_{ex}\vec{S}_i.\vec{S}_j$

Macroscopic Magnetization



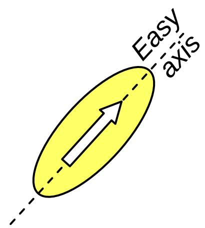
Ferromagnetic

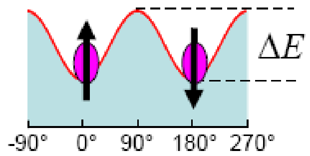


Antiferromagnetic

Lattice coupling
+ shape anisotropy

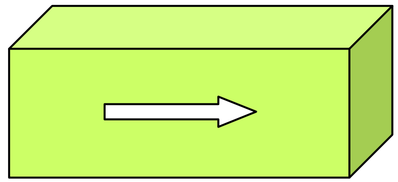
Magnetic anisotropy





$\Delta E = K_u V$

Permanent magnet

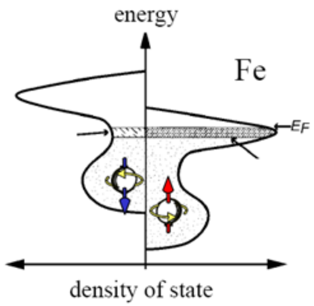


- Intrinsic logic system (2 states)
- Non volatile
- Size-independent

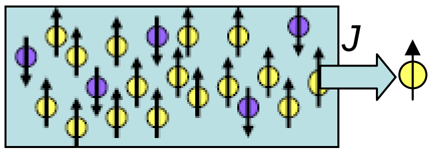
… as long as $\Delta E > k_B T$

SPIN TRANSPORT

Exchange interaction
→ Band splitting

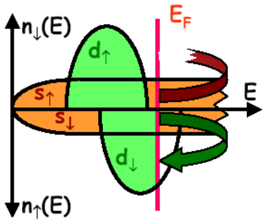


Spin polarized current in and exiting magnetic layers

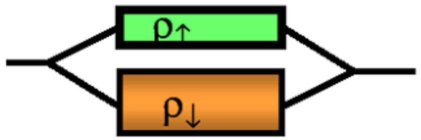


Sustained until spin-flipping diffusion event

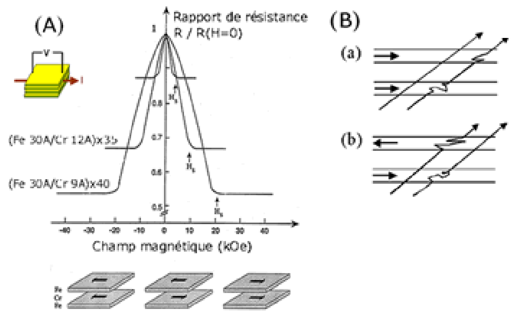
In metals, if spin flip marginal
→ Scattering proportional to available DOS just above E_F



Mobility (conductance) asymmetry

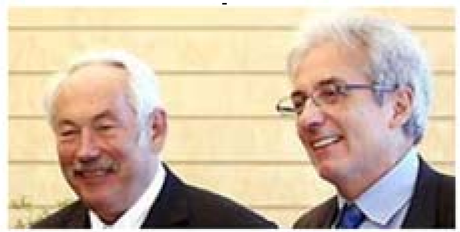


ρ depends on relative orientation of spin current and local $\vec{M}$



Giant MagnetoResistance (GMR)

2007
Nobel Prize



Dr.Gruenberg Prof. Fert

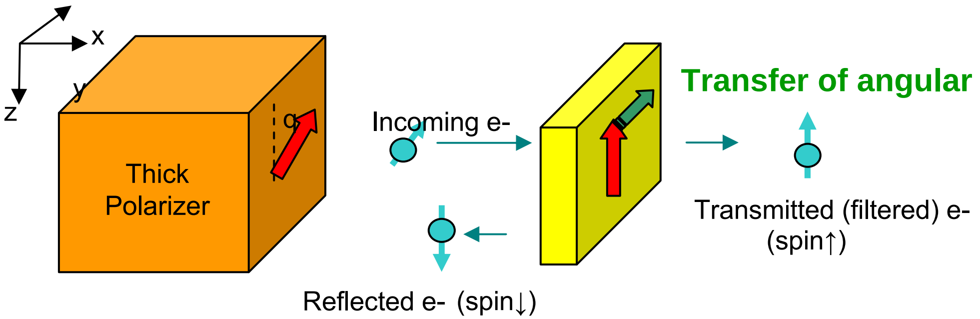
spintec
SPIN IN ELECTRONICS

cnrs inac INSTITUT NANOSCIENCES ET CRYOGÉNIE Grenoble INP

SPIN TRANSFER TORQUE (STT)

Magnetization → (Resistance) → Current ⇒ « Magnetoresistance »

(Spin) Current → Magnetization ⇒ « Spin Transfer Torque »

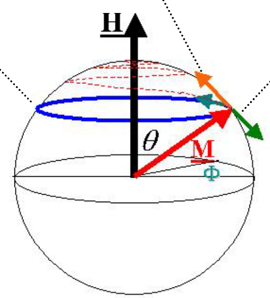


Transfer of angular momentum = STT

Extended Gilbert equation :

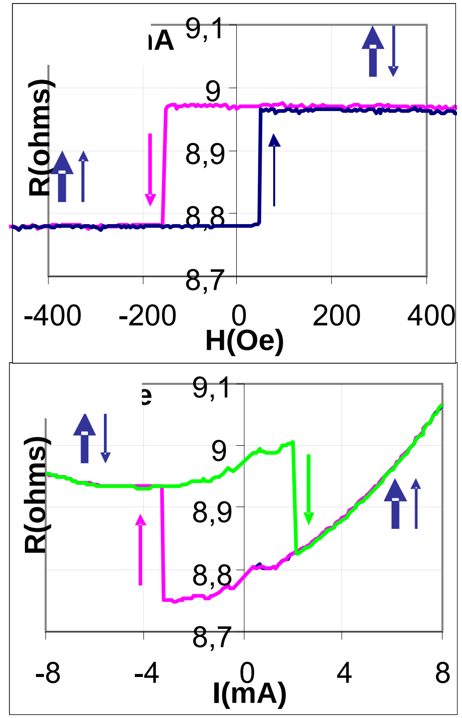
$$\frac{d\vec{M}}{dt} = -\gamma(\vec{M}\times\vec{H}_{eff}) + \frac{\alpha}{M_S}\vec{M}\times\frac{d\vec{M}}{dt} + \frac{\gamma a_J(\theta)}{M_S}\vec{M}\times(\vec{M}\times\vec{P}) - \frac{\gamma b_J(\theta)}{M_S}(\vec{M}\times\vec{P})$$

Precession **Damping** **Spin torque (ST)**

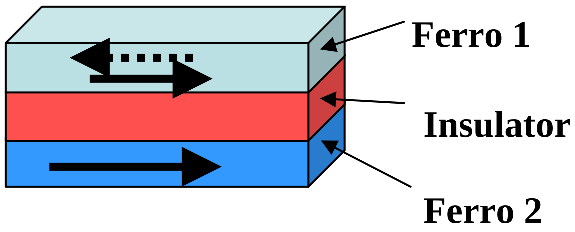


If spin torque < damping torque
➔ No switching

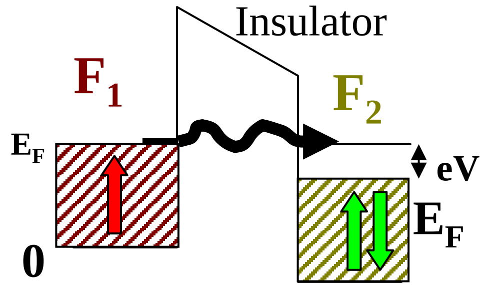
If spin torque > damping torque
➔ Switching



SPINTRONICS BUILDING BLOCK : THE MTJ

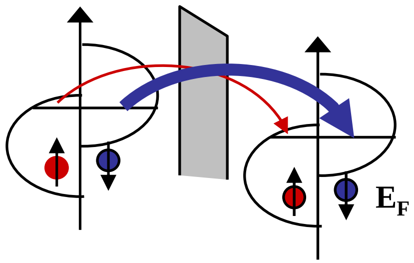


Magnetic Tunnel Junction



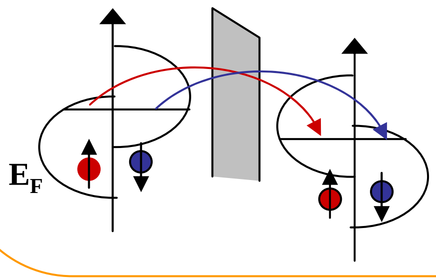
$$\sigma \propto n_1(E_F) \times n_2(E_F)$$

Parallel state

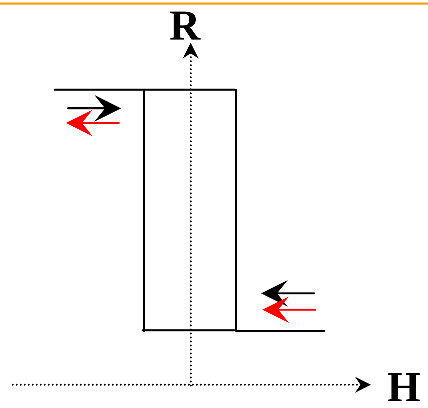


Low R

Antiparallel state



High R

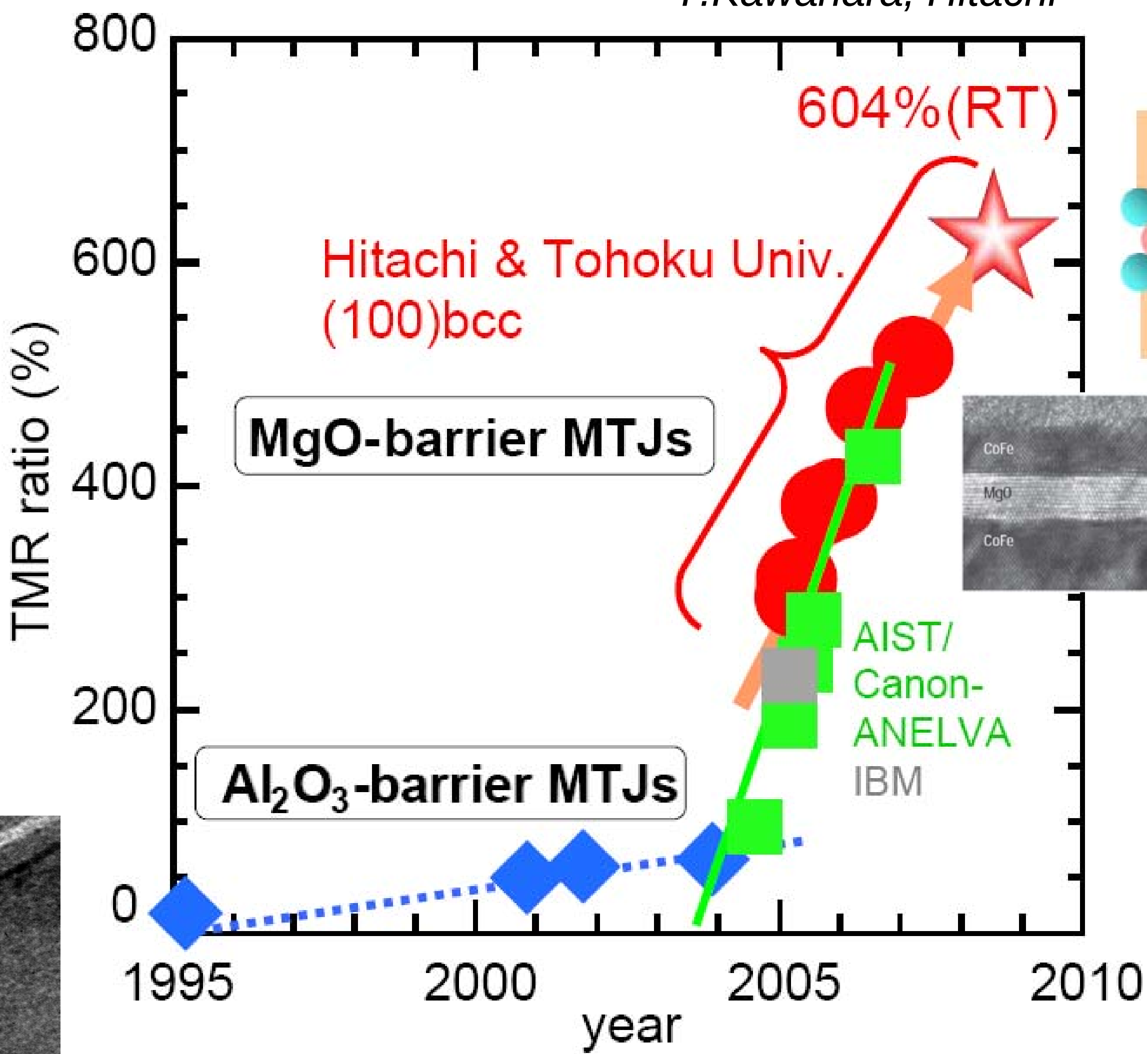


$$TMR = \frac{R_{\uparrow\downarrow} - R_{\uparrow\uparrow}}{R_{\uparrow\uparrow}}$$

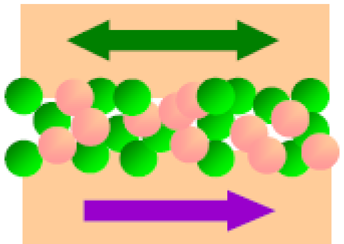
Tunnel Magneto-Resistance

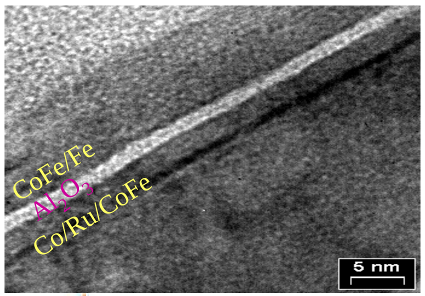
MRAM BUILDING BLOCK : THE MTJ

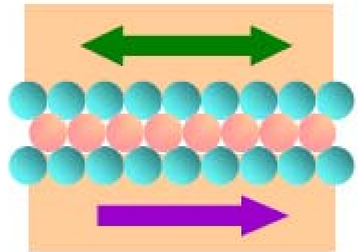
T.Kawahara, Hitachi

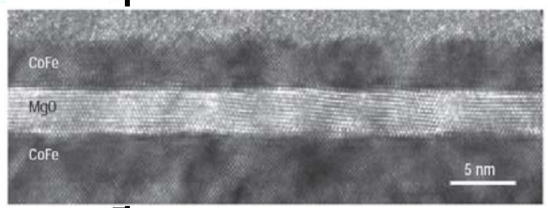


Amorphous :
Incoherent tunneling
of various Bloch states



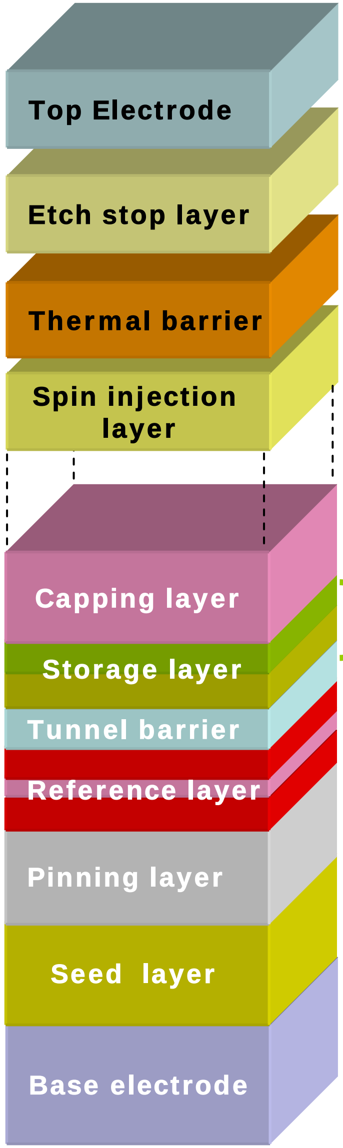






Crystalline:
Specific wave
functionsoverlap

MRAM BUILDING BLOCK : THE MTJ



Complex but mastered for volume manufacturing
(1 millions heads/day since 5+ years !)

Protects MTJ during process

NiFe(3) / CoFe(2) : Stores data (2 stable states)

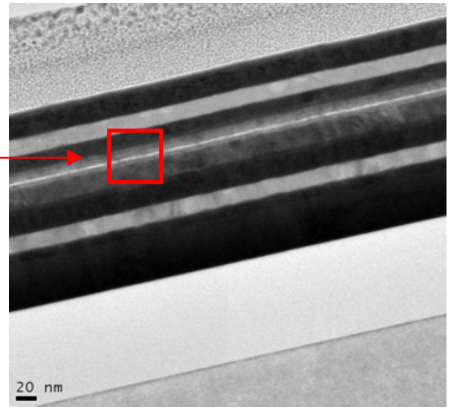
MgO (1.1) : Defines cell R & TMR

CoFeB(2) / Ru(0.8)/CoFe(2) : SAF, immune to external fields

PtMn(20) : AF layer sets direction of reference layer

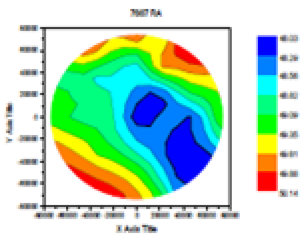
Ta(5) or NiFeCr(10) : Promotes texture of critical layers

Contact to select transistor
+ diffusion barrier



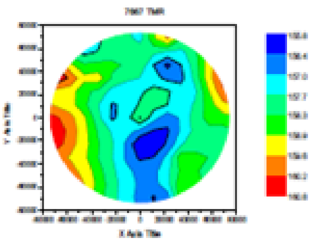
MTJ MANUFACTURING

RA

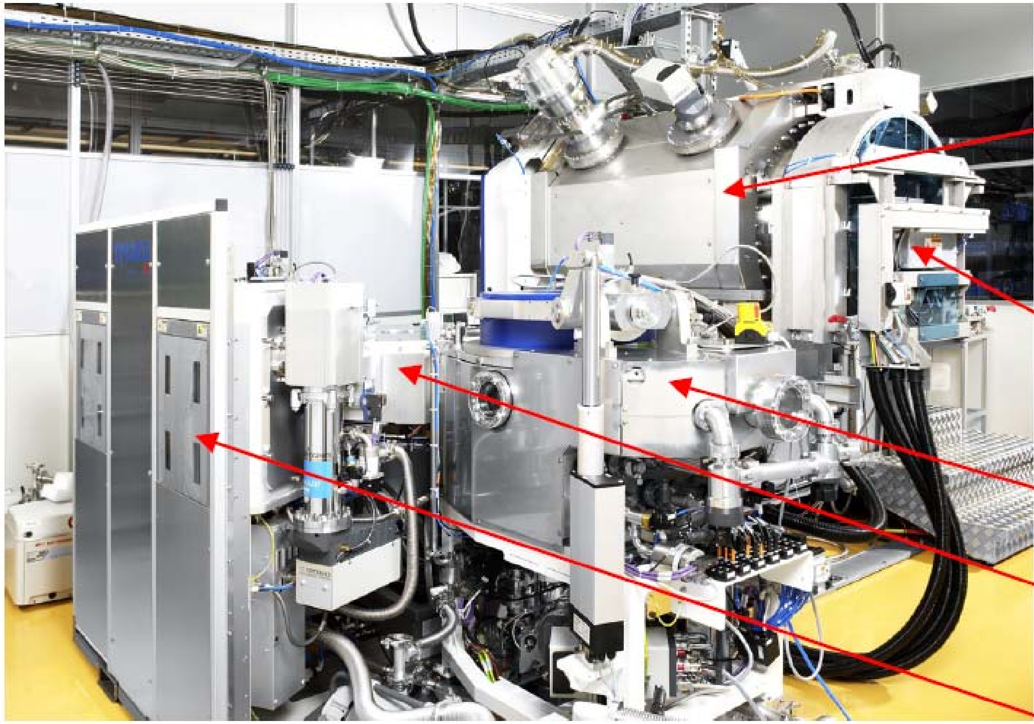


49.1 Ohm µm²
1.3% (1sigma)

TMR



158.2%
1.0% (1sigma)



Multi Target Module
Top: Target Drum with 10 rectangular cathodes; Drum design ensures easy maintenance;
Bottom: Main part of the chamber containing LDD equipment

RF – Equipment
(Match – Box,
RF - Switches)

Soft-Etch Module
(PreClean, Surface Treatment)

Transport Module
(UHV wafer handler MX700)

Cassette Modules
(according to Customer request)

Ultra – High – Vacuum Design:	Base Pressure ≤ 5*10^{-9} Torr (Deposition Chamber)
High Throughput:	≈ 10 Wafer/Hour (NiFe 2.5nm/CoFe70 250nm)
High Tool Availability:	Maintenance friendly Design
High Reliability:	Solid and Well Engineered Design → Up-Time: ≈90%, MTBF: ≈150h, MTTR: ≈ 3h

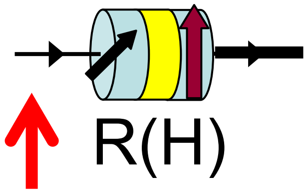
CROCUS Technology
Blossoming future

SINGULUS
NANO DEPOSITION TECHNOLOGIES

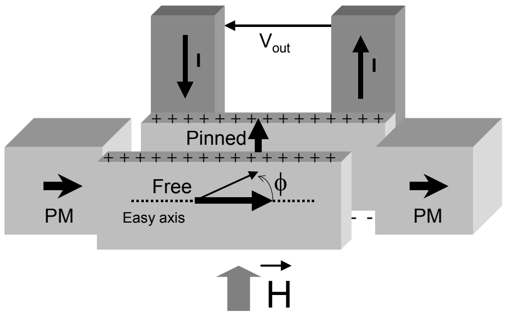
spintec
SPIN IN ELECTRONICS

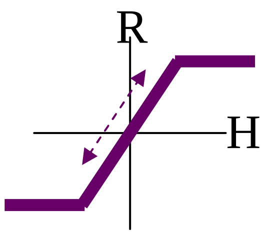
GMR/TMR SENSORS

External Field → Magnetization → Resistance

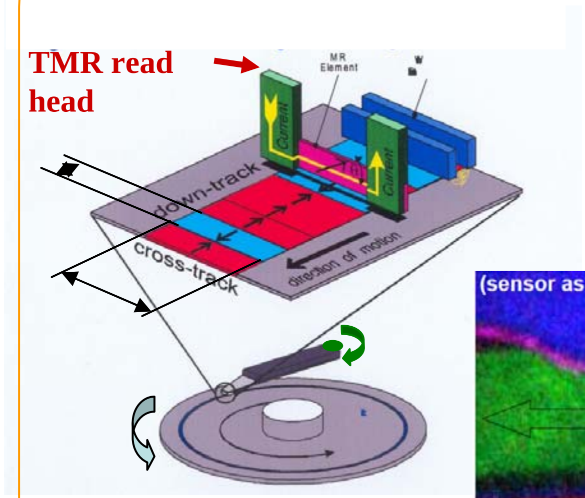


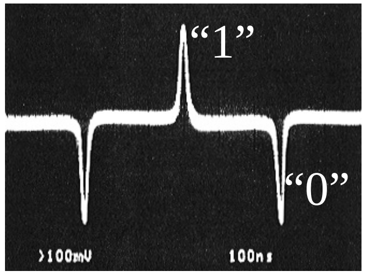
Position sensors
(earth field)

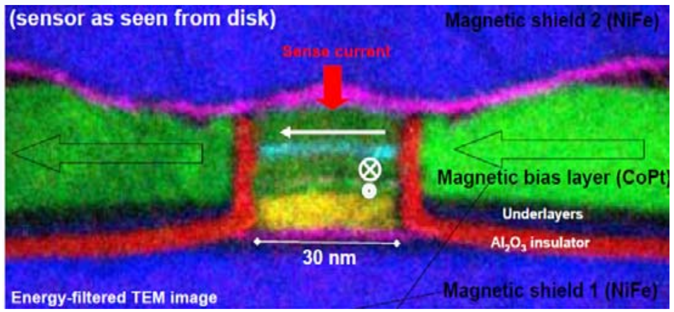




Disk drive heads
(media bits stray field)



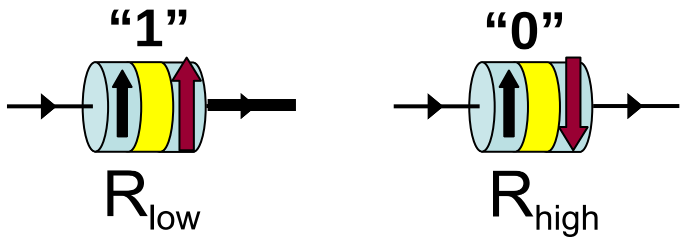


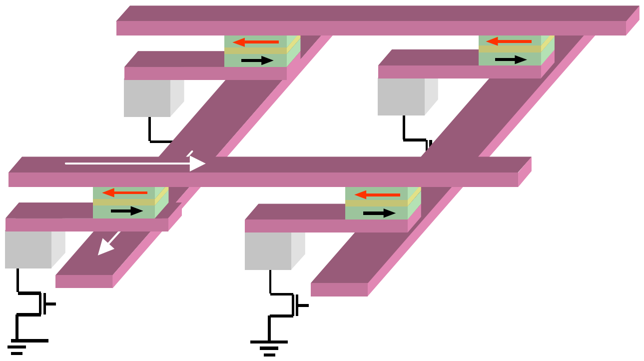


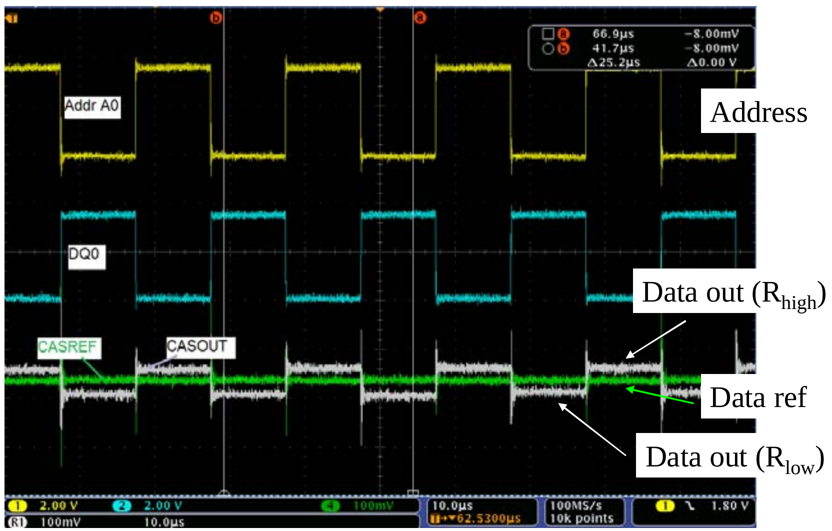
Peripheral (CMOS) circuit not integrated
Single element devices
Volume manufacturing on Si or AlTiC wafers
Sub-"30nm" technology

MAGNETIC RANDOM ACCESS MEMORIES

Magnetization state → Logic memory state







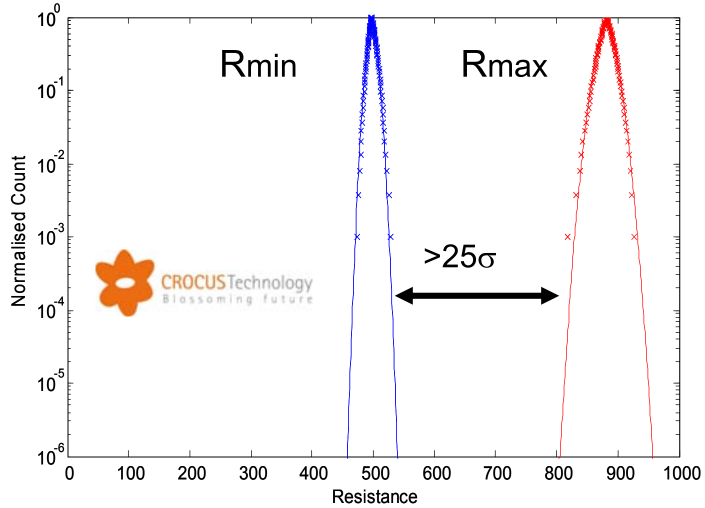


Figure of merit is not ΔR, but ΔR/σ

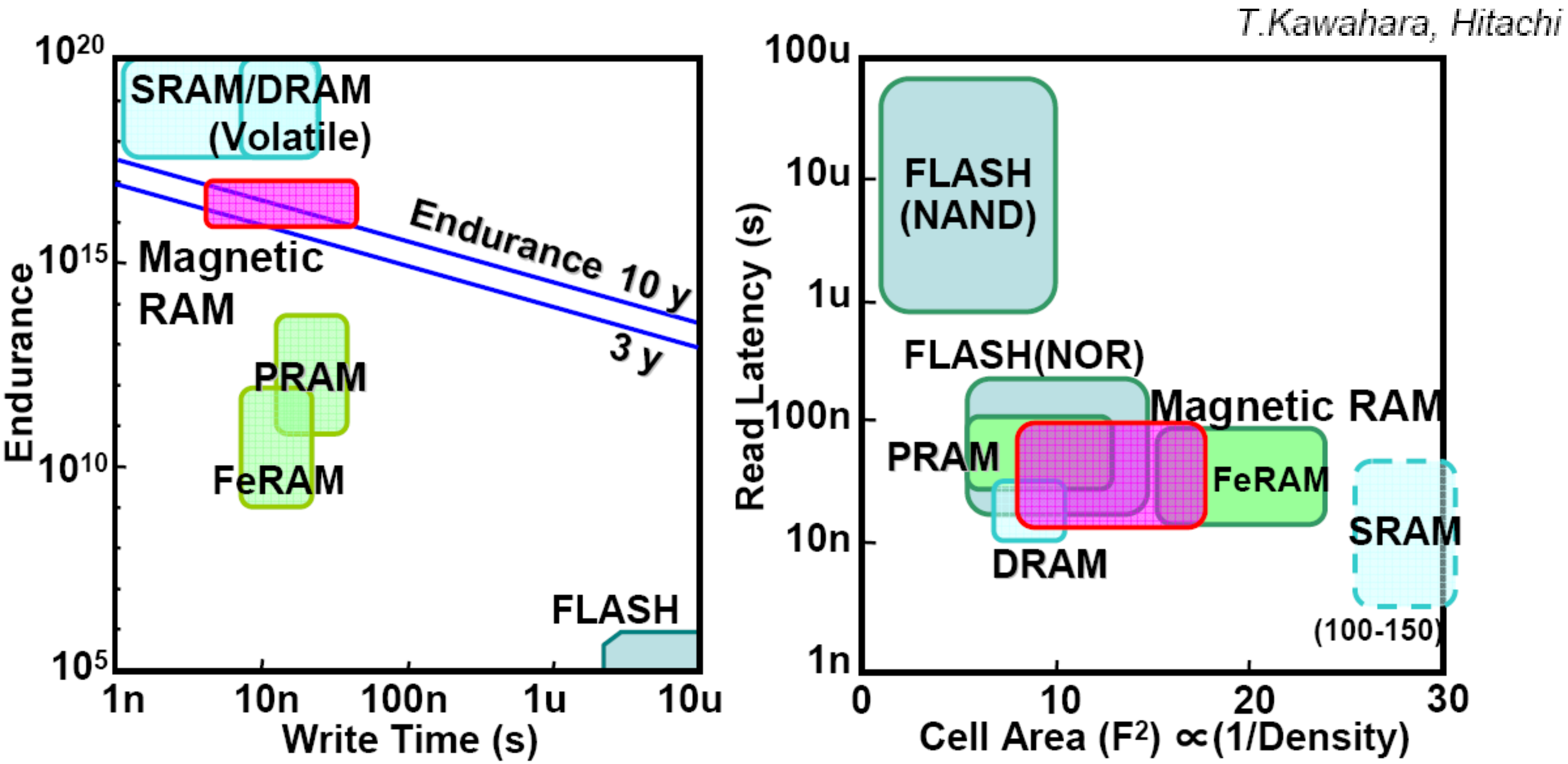
ΔR/σ >25 for functional device,

>40 for production-worthy process

WW distribution 1σ need to be < 1%

WHY MRAM ?

Although not the best in each category, MRAM is the only memory which scores everywhere

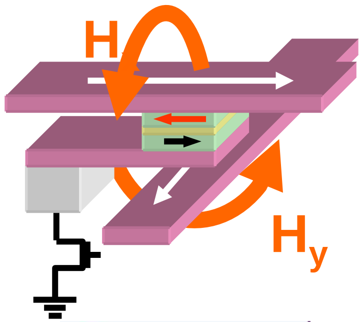


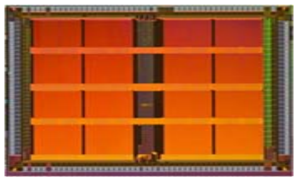
Fast, non-volatile, infinite endurance memory

+ moderate power (no HV), rad-hard, easy to embedd

THERE ARE MANY MRAM !

Field-only « Toggle »





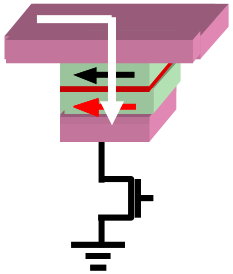
Freescale 4Mb (2006)

Established technology
1.5M units shipped
4.5M forecasted in 2011
Infinite endurance

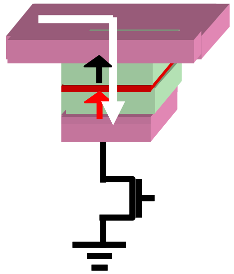
Scalability beyond 90 nm ?
(Write power increase)

Spin Transfer Torque « STT » or « SPRAM »

Planar



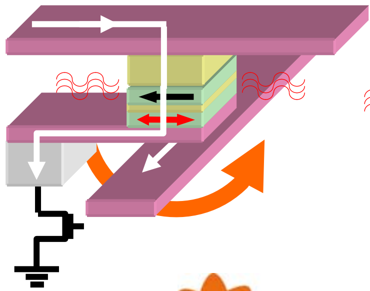
Perpendicular



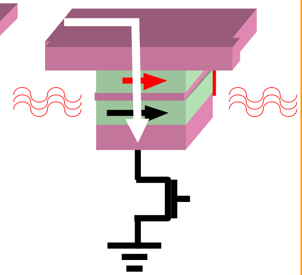
Lowest write current
(<100µA, scales with shrink)
Minimal cell / array size
(~15F², soon not Xtor limited)
Low sensitivity to field disturb
Beware of stability
(retention at small feature s

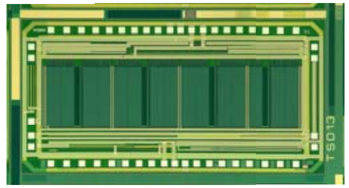
Thermal Assist « TAS » or « TAMRAM »

Field-TAS



STT-TAS





1Mb Field-TAS (2011)

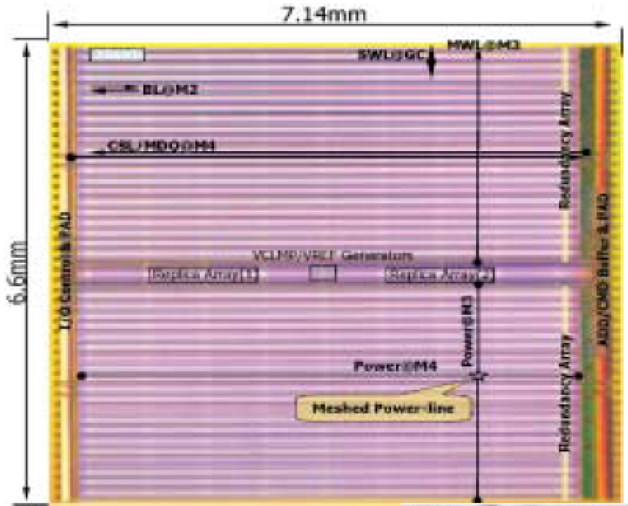
Fully scalable
(stability / retention to <20nm)
Multibit possible
Limited array efficiency
+ large field drivers)

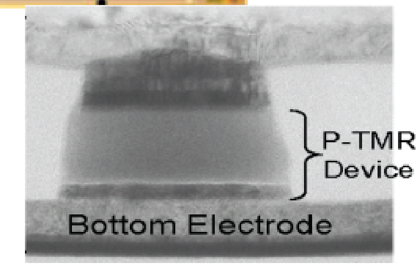
Combine both !

LATEST DEMO CHIPS

Perpendicular TMR (Toshiba)

- Process: 65 nm
- Power Supply: 1.2 V
- Density: 64 Mb
- Chip size: 47.12 mm^2
- Cell size: 0.3584 μm^2 (84.8F^2)
- Write Current: 50 uA
- TMR device: Perpendicular

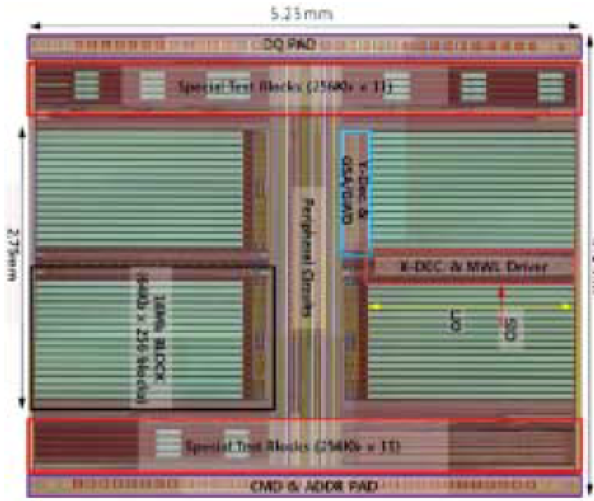


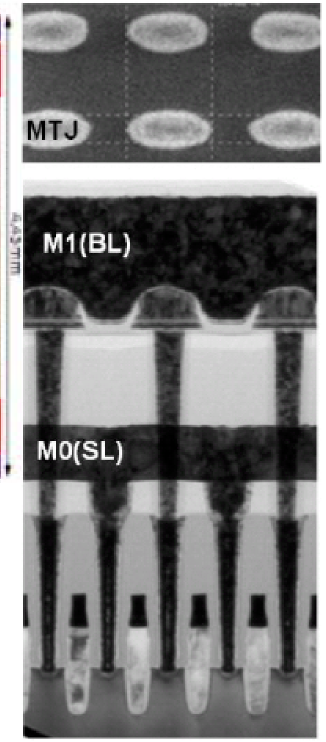


K. Tsuchida, et al., ISSCC 2010

Modified DRAM Process (Hynix, Grandis)

- Process: 54 nm
- Power Supply: 1.8 V
- Density: 64 Mb
- Chip size: 23.36 mm^2
- Cell size: 0.041 μm^2 (14F^2)
- Write Current: 140 uA
- TMR device: In-plane





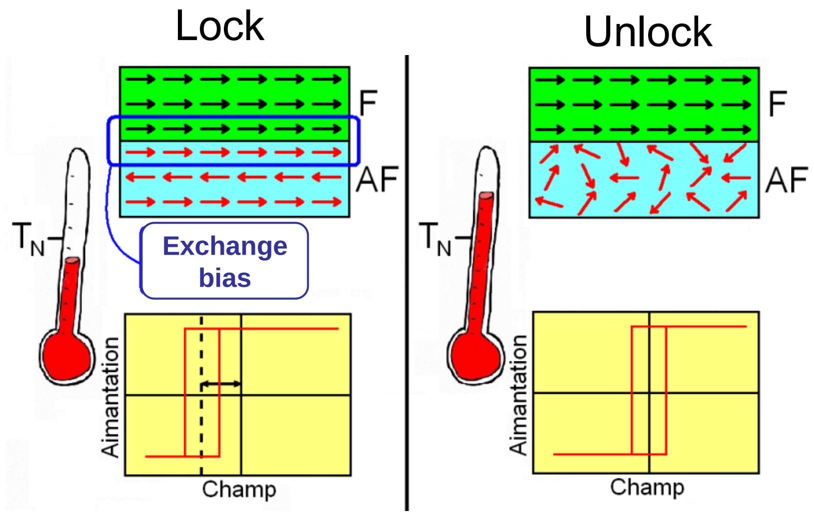
S. Chung, et al., IEDM 2010

TAS MRAM PRINCIPLE

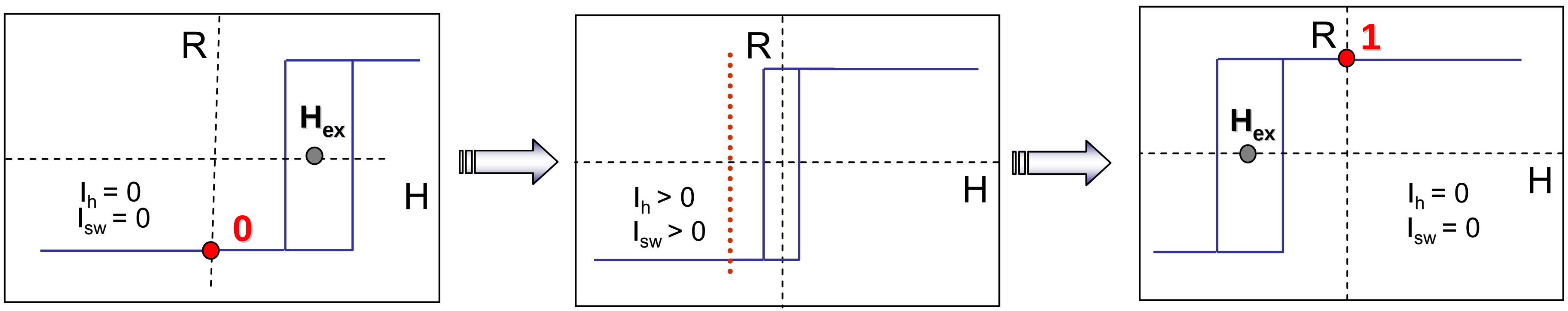
❖ Use **exchange biased bilayer** to "lock" the stored data (**high stability)**

❖ **Heat the cell** above to "unlock" the data

❖ Analogous to Heat Assisted Recording in HDD (write at elevated T, store at RT)



TAS write sequence



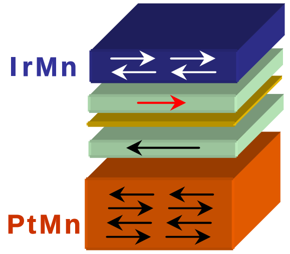
T = ambient temperature | **T > blocking temperature** | **T = ambient temperature**

Step 1: Heat cell by flowing current through transistor

Step 2: Switch magnetization by a **magnetic field or STT** torque

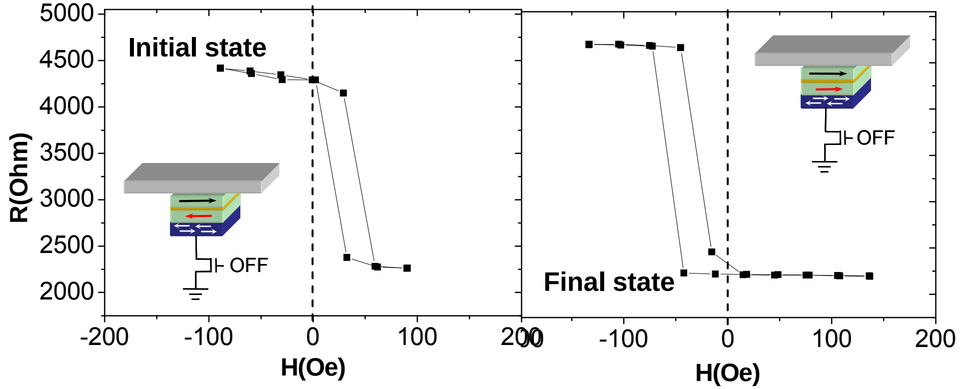
Step 3: Cool under magnetic field or STT torque

STT + TAS PROOF OF CONCEPT

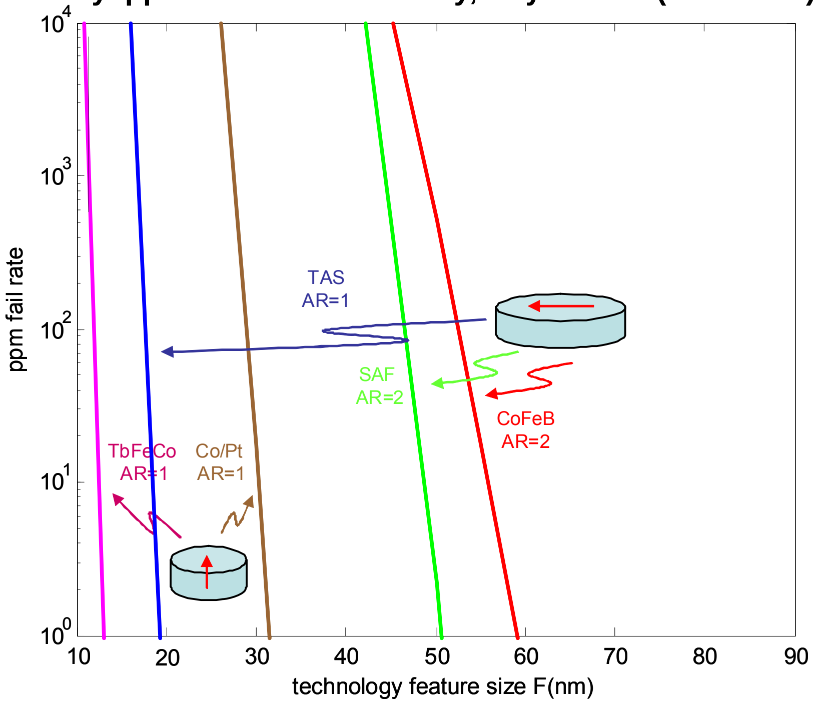


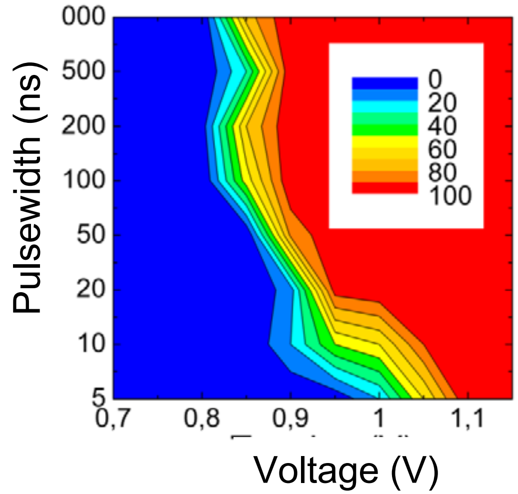
TAS-Field MTJ stack

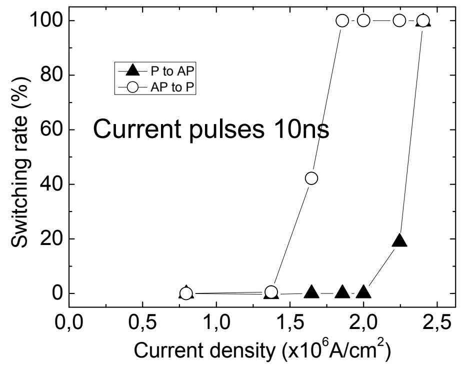
- ❖RxA from 30Ωµm² to 10Ωµm²
- ❖ TMR up to 130%
- ❖ Cell size 50nm (circular)



10yr ppm fail rate in 32M array, 10 years life (calculated)





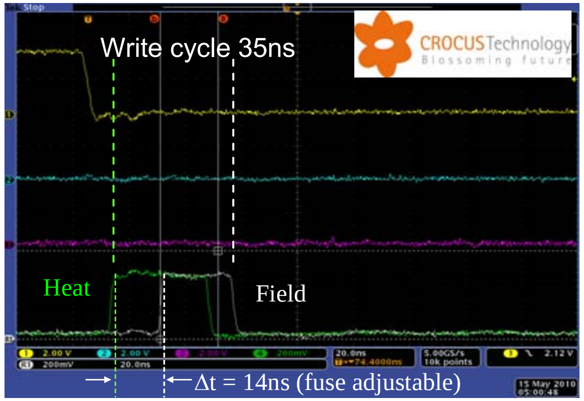


- ❖ Current density @ 10ns **Jc = 2.4 10⁶ A/cm²**
- ❖ **KV/k_BT > 100** at 32nm feature size (AR=1)

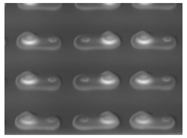
spintec SPIN IN ELECTRONICS leti

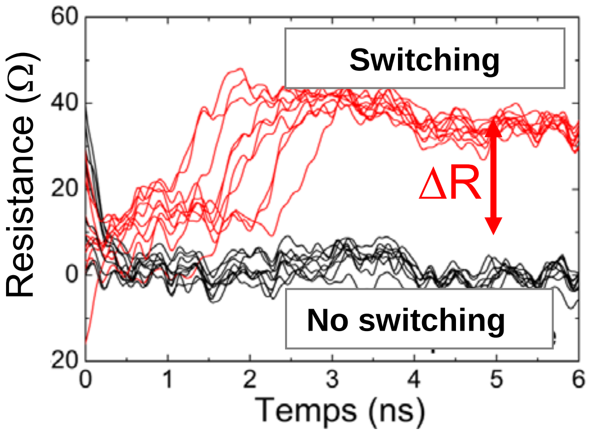
HOW FAST CAN MRAM BE ?

Field MRAM

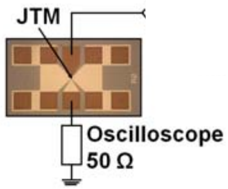


Chip level



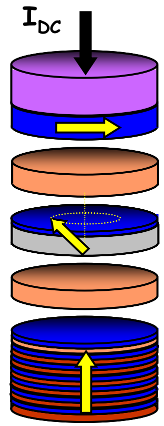


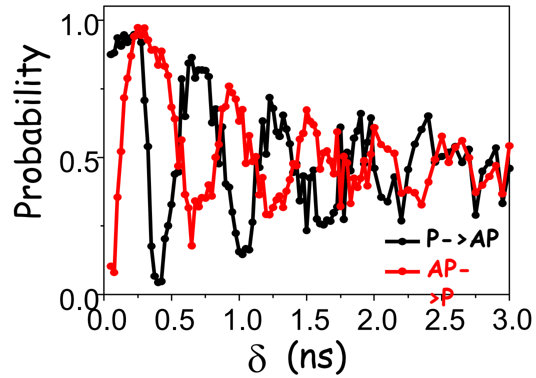
Real-time dynamic test



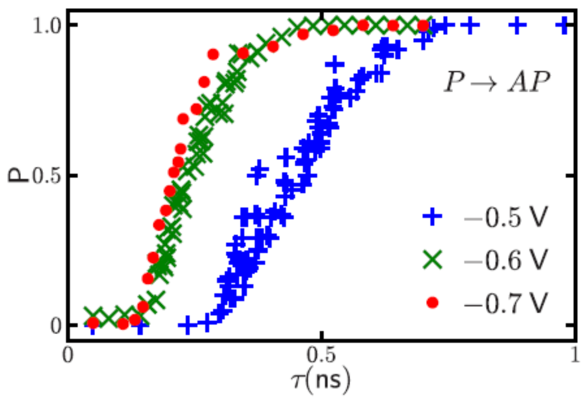
Switching transient ~ 1 ns
Switching time 5-10 ns (thermally activated)
Product Write cycle ~30 ns

STT Precessional switching





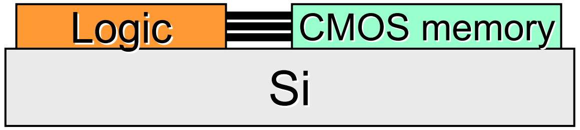
H.Liu et al, APL97, 242510 (2010)



Switching transient ~ 200 ps
Switching time < 1ns (deterministic)
Expected Write cycle ~2-3 ns

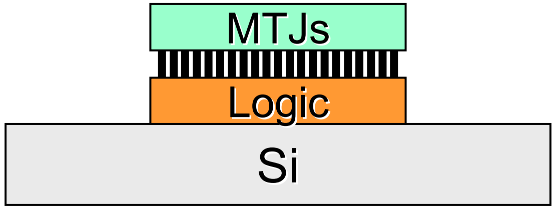
(MAGNETIC) LOGIC-IN-MEMORY

Von Neuman SoC



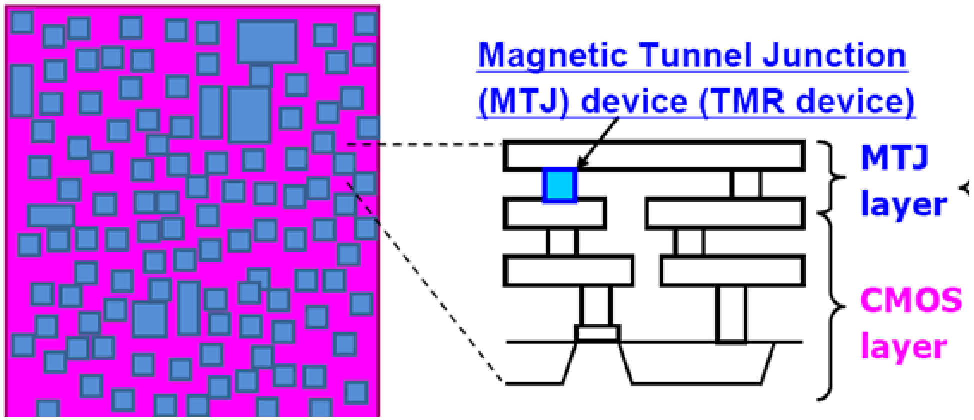
Large Si footprint, long interconnects
→ Delay, capacitive loss, complex layout, heat

"Janus" SoC



Minimal Si footprint, short interconnects
→ Faster, simpler layout, reduced dynamic power

Logic-in-memory concept (introduced in 1969)
Storage elements are distributed over the logic plane
Non volatility directly inside the logic circuit



Non volatile memory
→ No leakage
→ Static power off

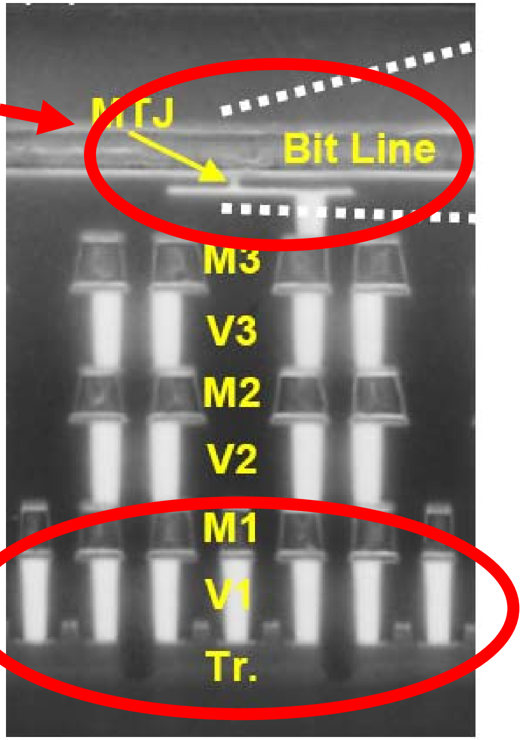
Reduced wire count
→ Minimal dynamic power, delay
Optimal layout

T.Hanyu, Tohoku University, 1th Joint MMM-Intermag Conference, Jan. 21, 2010

Need NV, fast, infinite endurance, CMOS compatible memory !

MTJ-BASED LOGIC CIRCUITS

- Infinite endurance (>10^{16} for field write)
  High speed (1-30ns)
- Cell R adjustable, from Ω's to MΩ's
  → Match with CMOS (~ kΩ)
- Cell is variable resistance driven by low voltage
  → use as standard library IP
- Can be deposited on any substrate
  → ''end-of-back-end » » process (above-IC)
  no impact on logic process
  only 3 add-masks



Front-end contamination under control

Low-T BE process (250°C) compatible with Cu interconnect process

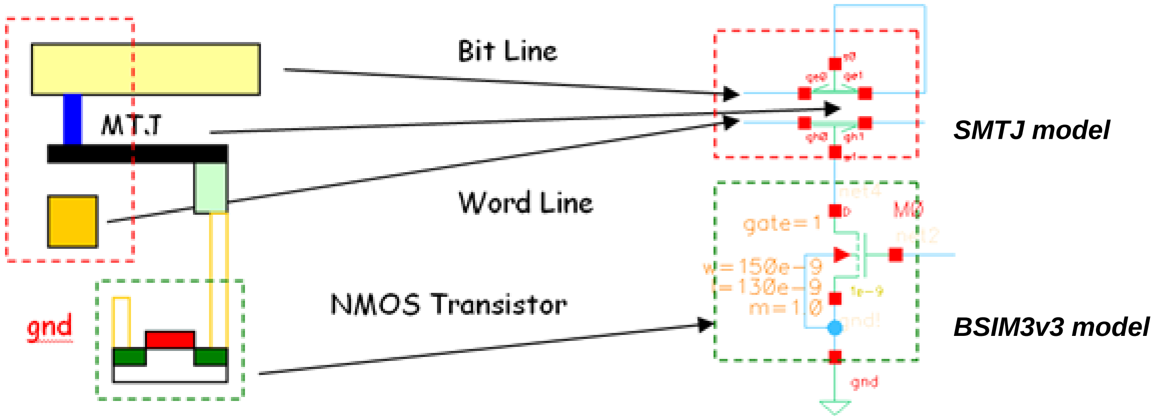
Etch still « tricky » → IBE vs. RIE ?

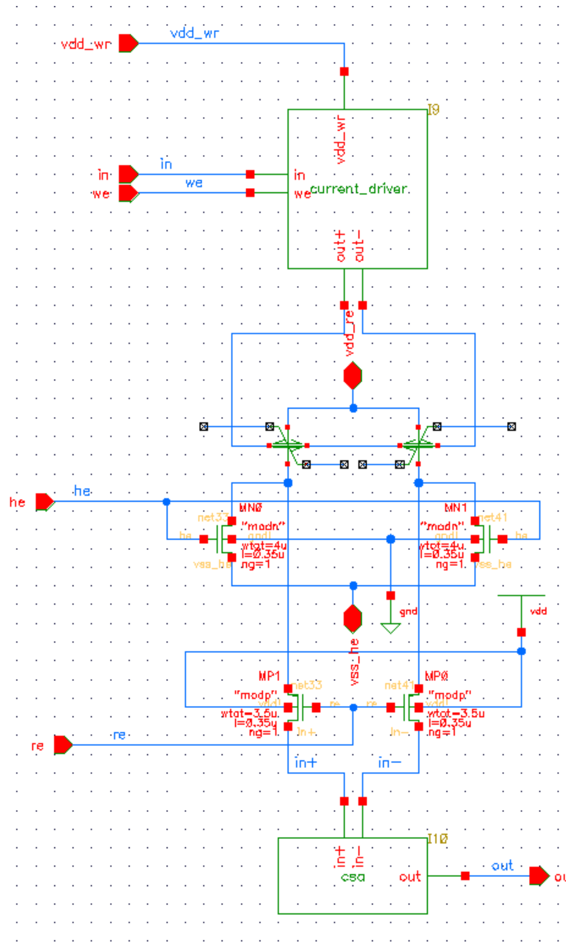
MRAM process well established
Fear for contamination (slowly) vanishing
Several fabs now enabled with 200/300mm lines

MTJ ELECTRICAL COMPACT MODEL

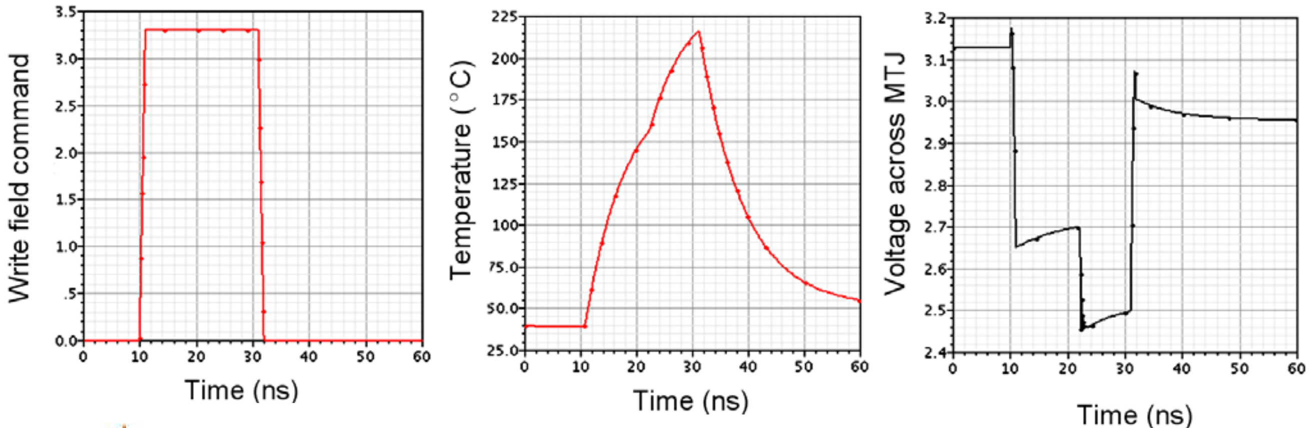
High-Speed compact model → Electrical behavior of MTJ written by field, STT and with/without thermal assistance.

SPECTRE (5.0) compatible (CADENCE platform analog solver).





Simulation of a TAS-MRAM



(MAGNETIC) NV-LOGIC CIRCUITS

Hitachi + Tohoku University

S.Matsunaga et al, Applied Physics Express, vol. 1, 2008.

- NV-Full Adder
  - One input is made non-volatile (instant startup, security)
  - Drastic static consumption reduction
  - Footprint reduction
- Demonstrator : CMOS 0.18µm,
- MTJs size: 200X100nm²

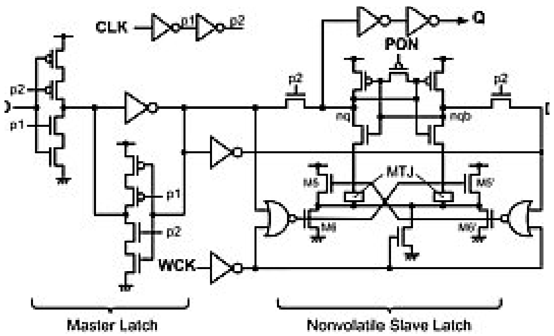
	CMOS	Hybrid
Delay	224 ps	219 ps
Dynamic Power	71.1 µW	16.3 µW
Writing Time	2 ns/bit	10 (2) ns/bit
Writing Energy	4 pJ/bit	20.9 (6.8) pJ/bit
Standby Power	0,9 nW	0 nW
Surface	333 µm²	315 µm²

NEC Empowered by Innovation

Home

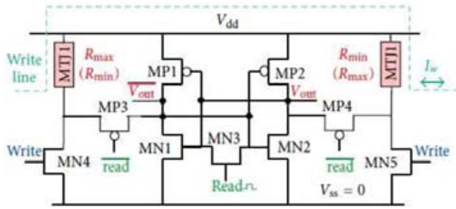
Home > News Room > NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs

NEC develops a nonvolatile magnetic flip flop that enables standby-power-free SoCs



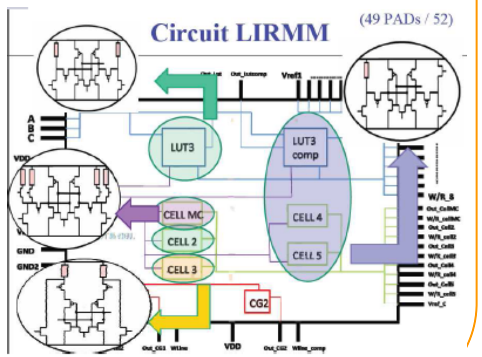
spintec

R-SRAM ©



Magnetic Flip-flop

Magnetic LUT



REPROGRAMABLE (MAGNETIC) LOGIC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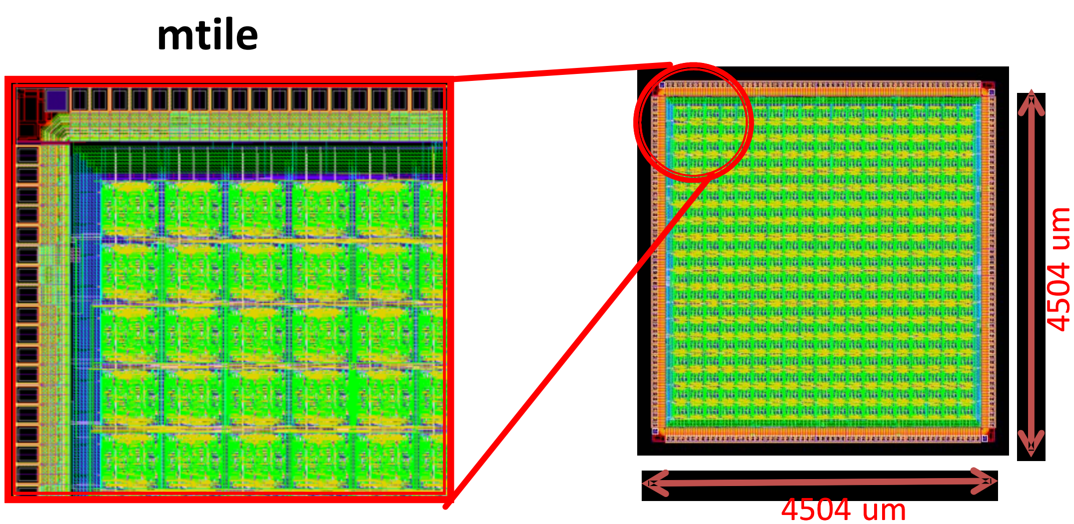
Press Releases

09-06-10 08:39

Menta and LIRMM Launch Manufacturing of World's First MRAM-based FPGA

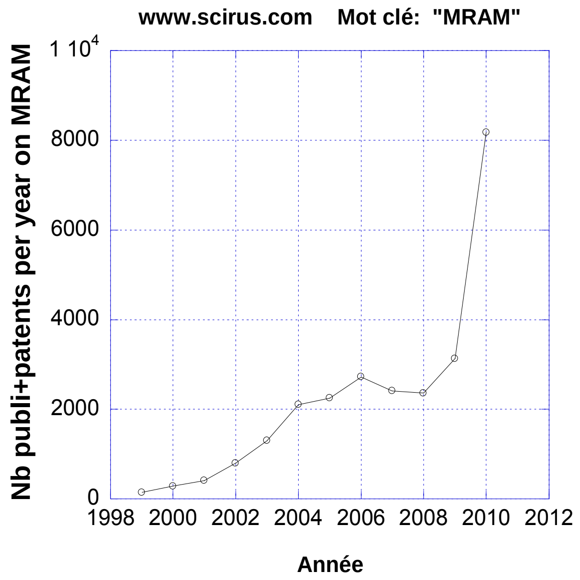
MONTPELLIER, France, June 9, 2010 — Menta SAS and LIRMM, an embedded programmable logic provider of embedded-FPGA Intellectual Property (IP) and a joint CNRS and University of Montpellier 2 research laboratory, today confirmed the tape out of world's first MRAM-based FPGA. The MRAM-based FPGA leverages key innovations including non-volatile magnetic memory and patent-protected circuitry enabling compact integration of MRAM and embedded-FPGA solutions.

# LUT 4	1444
# TILES	361 (19x19)
# Sequential elements	1444
# of MTJs	187 720
# of Transistors	$9.\ 10^6$
Silicon Area	$21mm^2$
MRAM Reconfiguration Tile Energy	9 nJ
MRAM Restoration Tile Energy	25,5 pJ
Clock Frequency	100 MHz
Full configuration time	72us + 93K Clock cycles
Tile reconfiguration	200ns + 260 Clock cycles
# Input/Output	76 Input / 76 Output

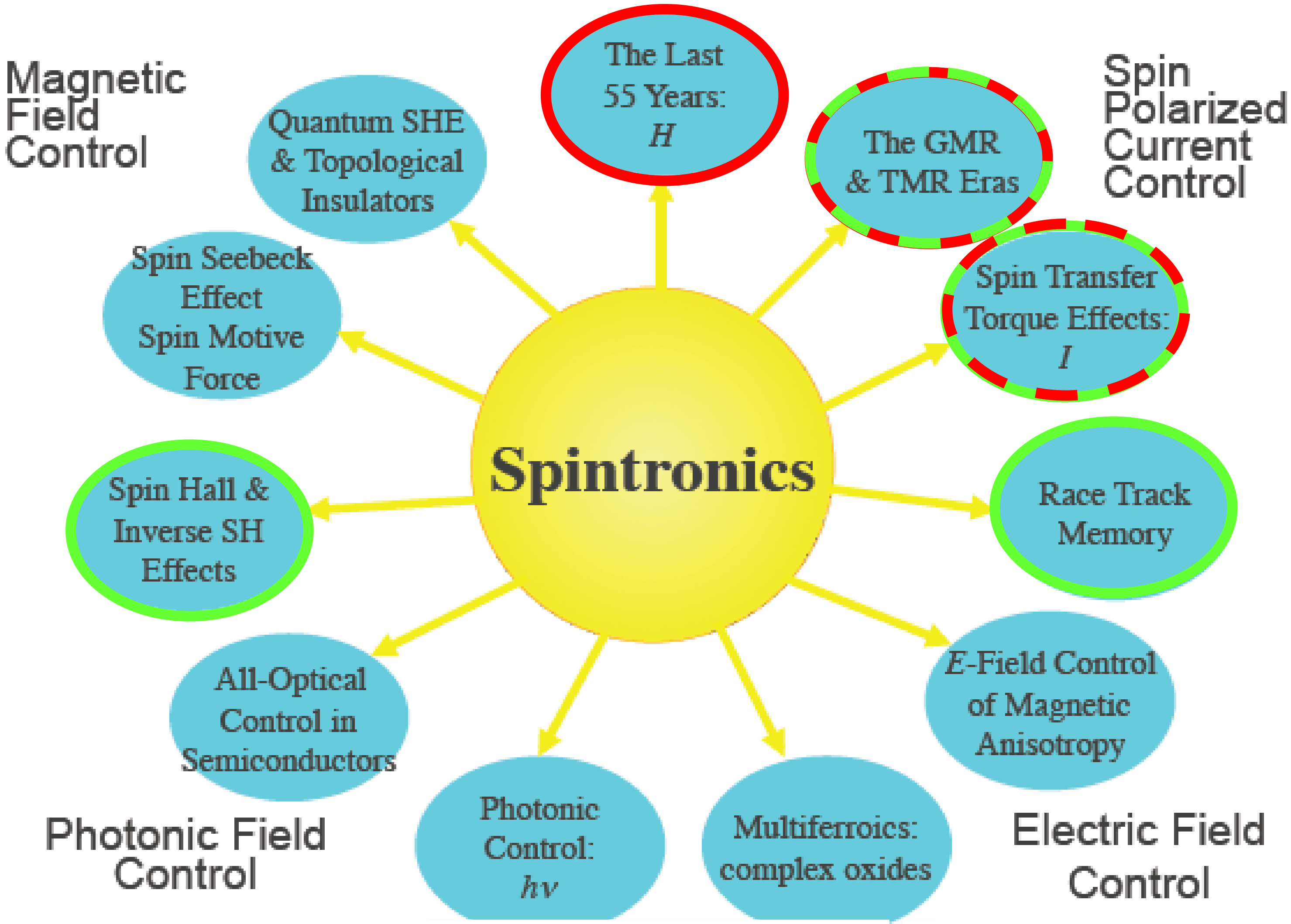


(INTERMEDIATE) CONCLUSION

- Increasing interest for MRAM for stand-alone, embedded memories or “logic-in-memory”
- Spintronics brings non volatility to CMOS circuits for low-power, normally-off electronics
- Manufacturing technology mature enough with pure-play foundries entering the game
- Design environment “ready-to-use” as standard library tools

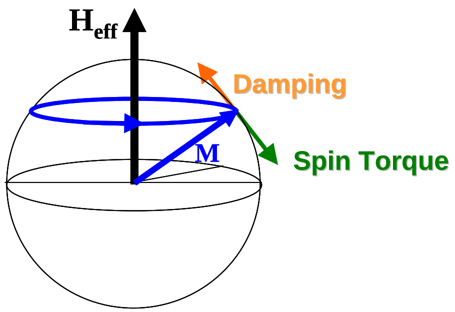


WHAT'S NEXT ?

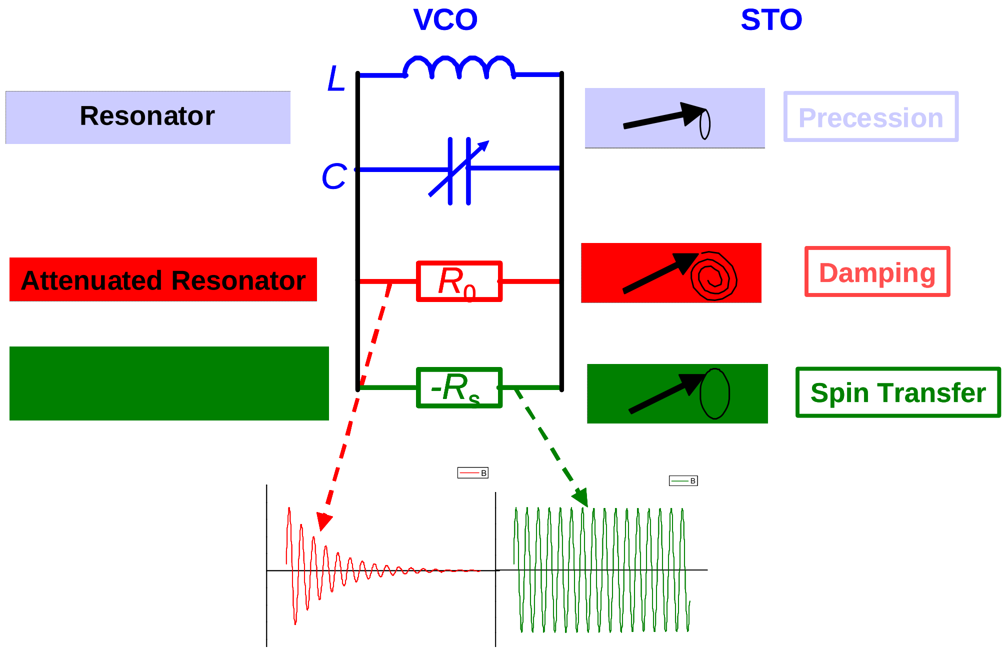


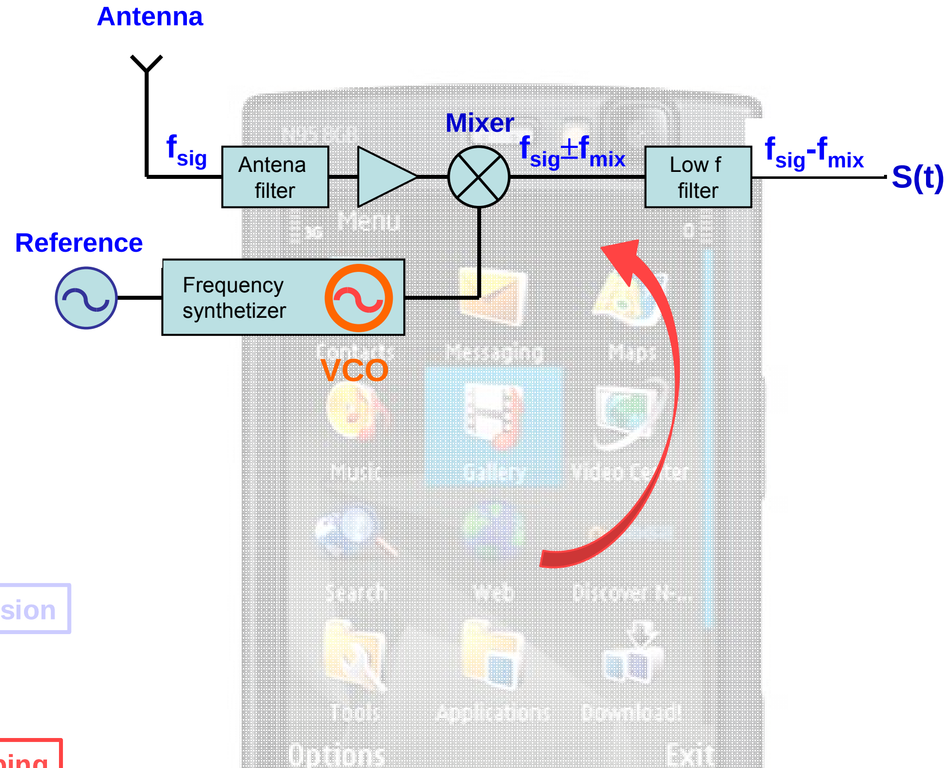
Courtesy Sam Bader

SPIN TRANSFER OSCILLATORS (STO)



If damping = STT → Self-sustained precession
→ Oscillations of R

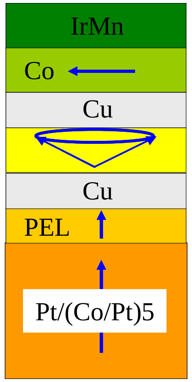


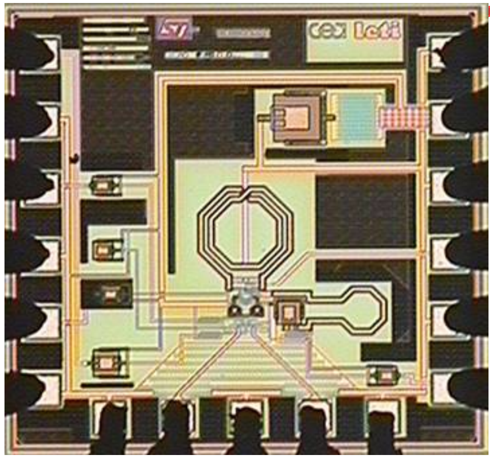


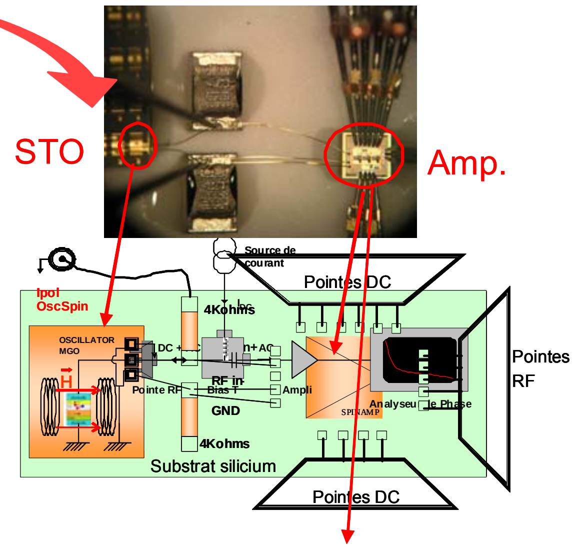
Resonnance frequency 1-40 GHz
Tunable by current and/or field
→ Radio-opportunism

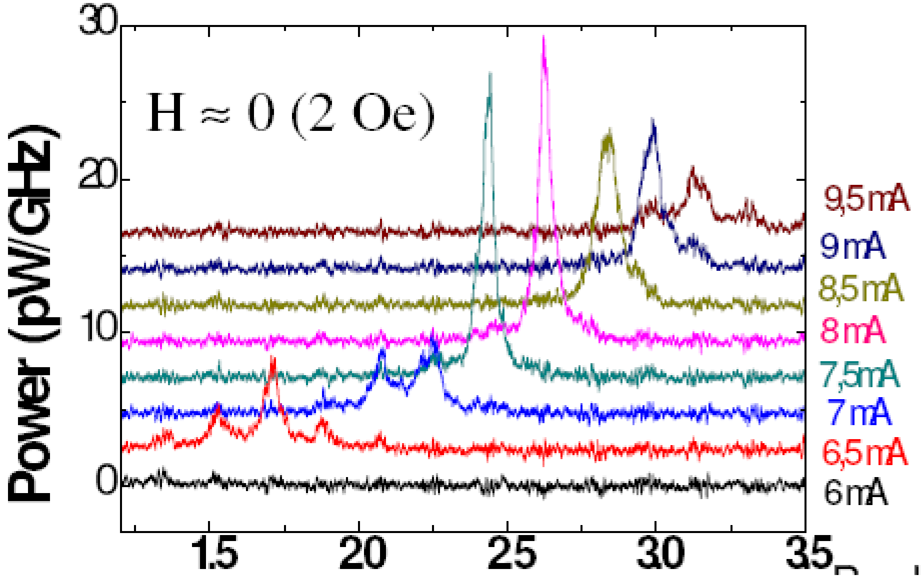
Can spintonics-based device replace VCOs in a transceiver chain ?

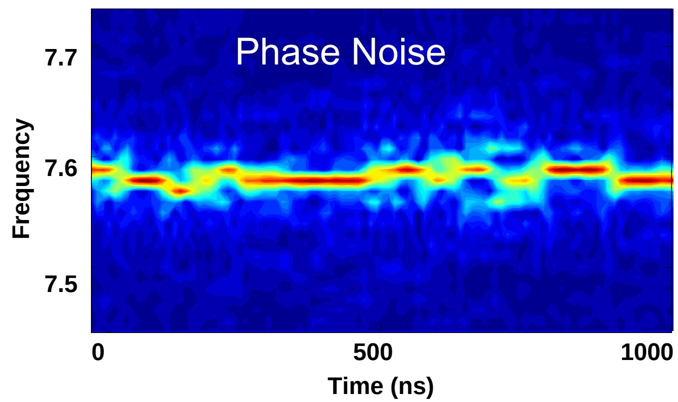
SPIN TRANSFER OSCILLATORS (STO)







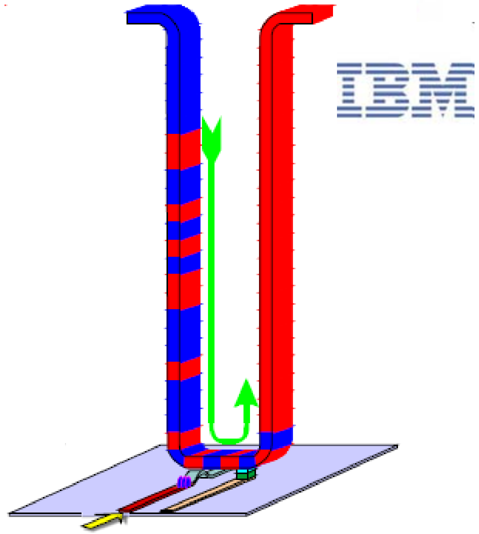




SPIN TRANSFER DOMAIN WALL MOTION

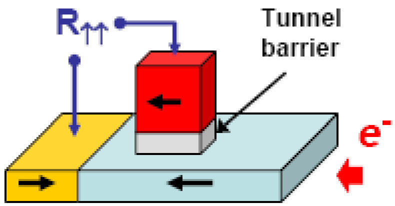
In Domain Wall, local "magnetic" pressure induced by STT ➔ DW motion

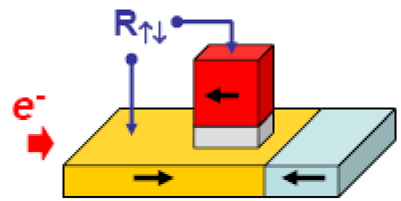
"Race Track Memory"

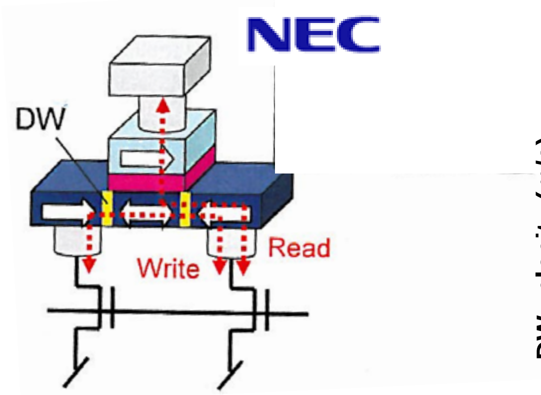


Magnetic shift register

MRAM & logic devices

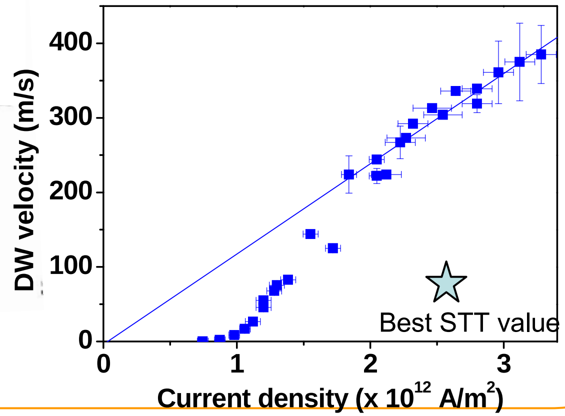






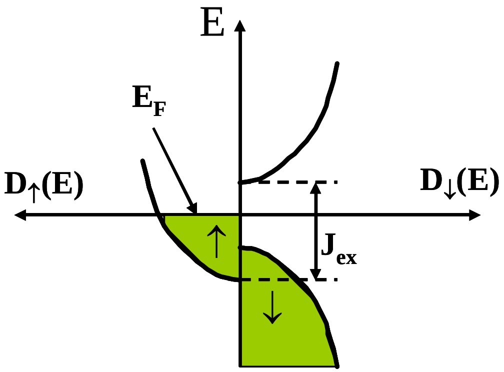
Rashba-induced DW motion in ultra-thin Pt/Co/Al_2O_3 layers

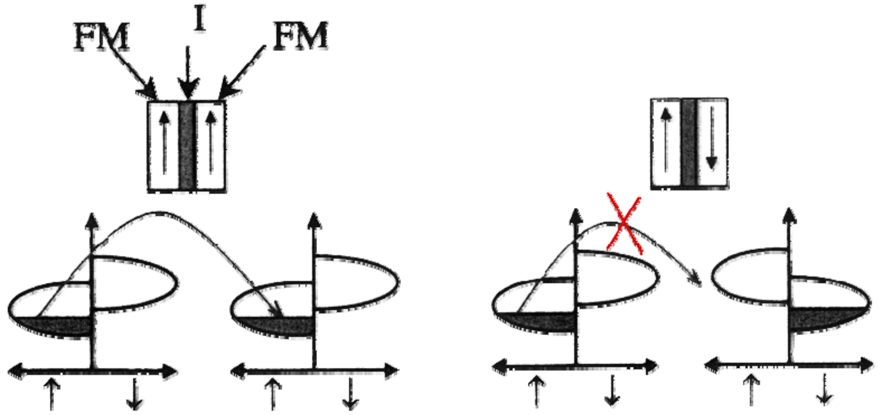
Nature Materials Vol.9,pp.230–234 (2010)



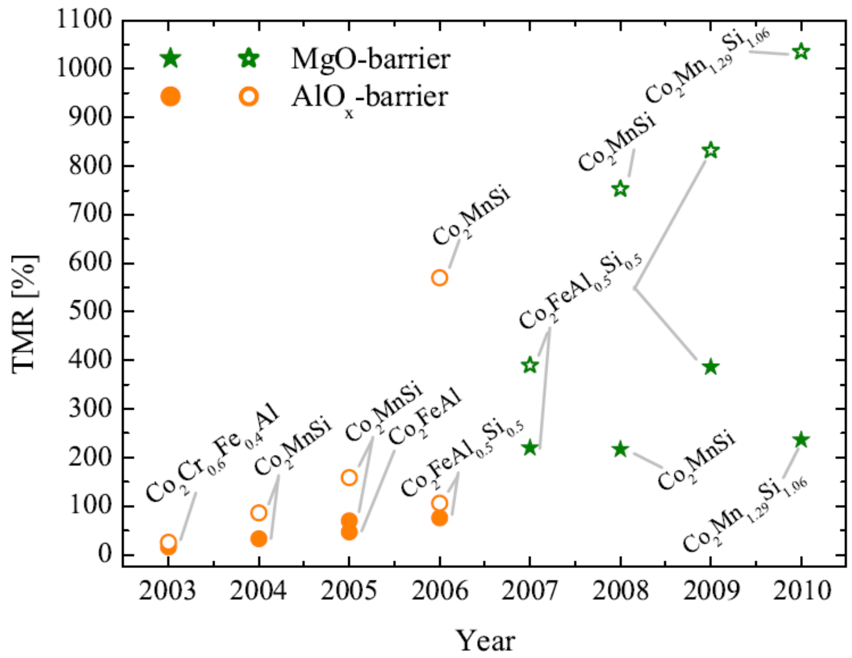
NEW MATERIALS : HEUSLER ALLOYS

Use « half »-metals (Heusler alloys)



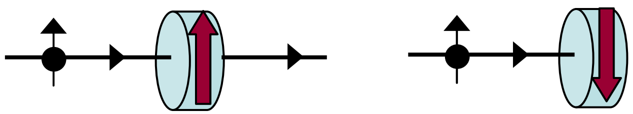


$$TMR = \frac{R_{antipar} - R_{par}}{R_{par}} \rightarrow \infty$$



Integration of half-metals could open the door for spin switches

→ Active logic devices



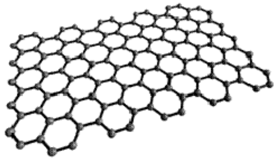
TOWARDS PURE SPIN LOGIC ?

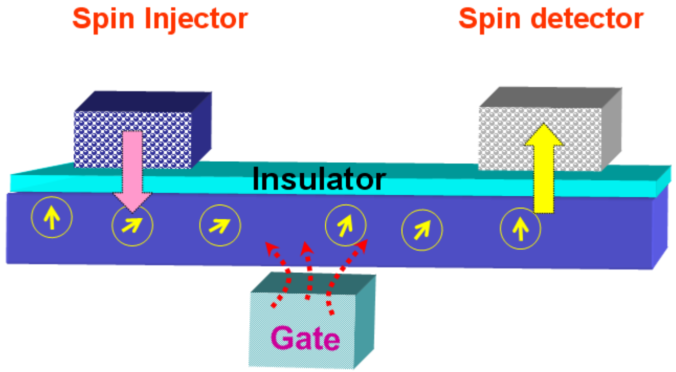
The long quest for a spin transistor …

Problems:

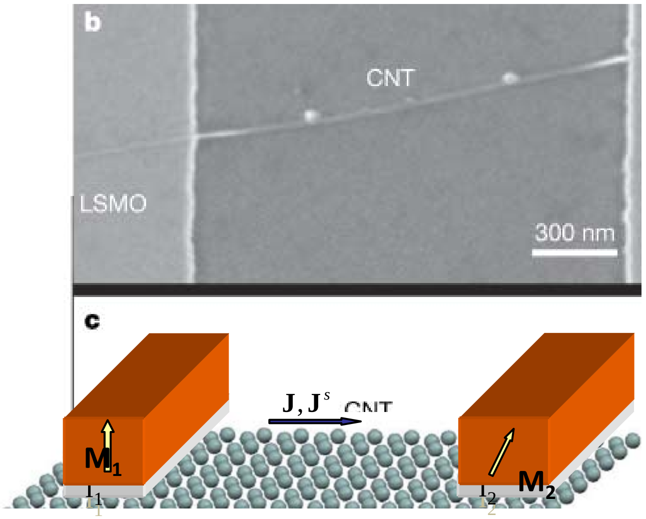
- No efficient spin injection from FM into SC
- Short spin lifetime in SC
- No magnetic SC at RT

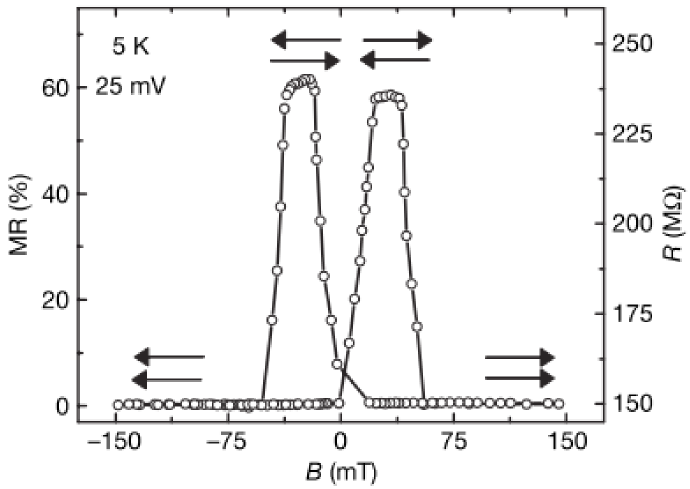
↳ Graphene Spintronics





L.Hueso, N.D. Mathur, A.Fert et al, ***Nature* 445, 410, 2007**



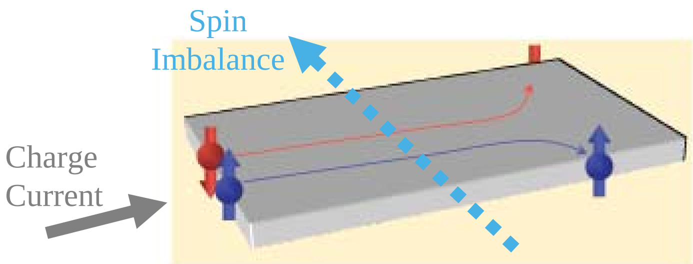


Extremly long lifetime + Efficient spin injection

SPIN-ONLY CURRENTS

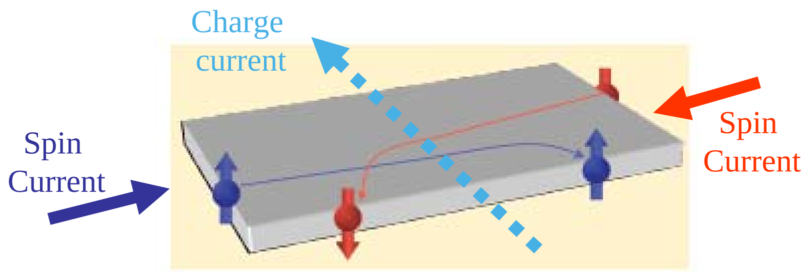
Spin-Hall

Charge current → Spin « current »

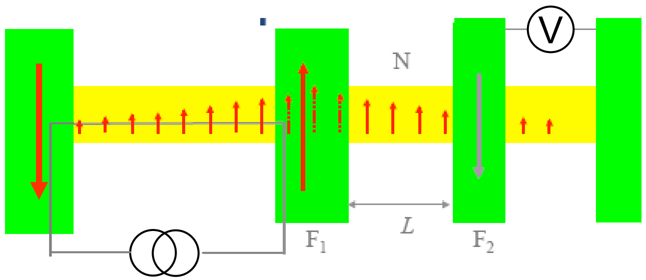


Inverse Spin-Hall

Spin current → Charge current

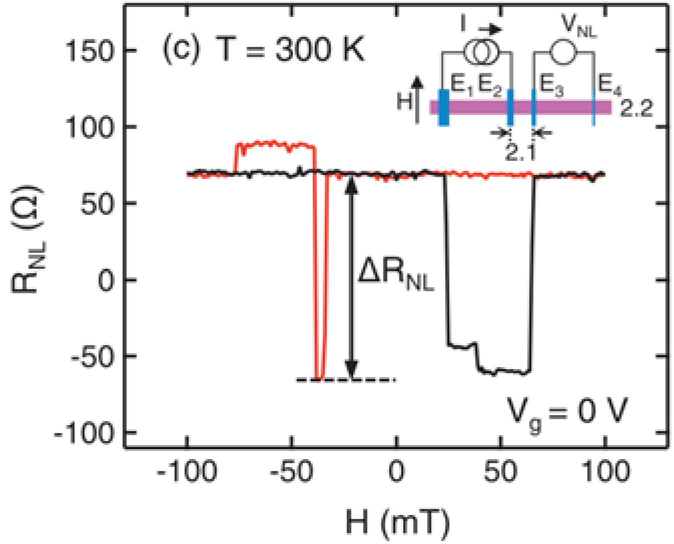


Spin injection into graphene



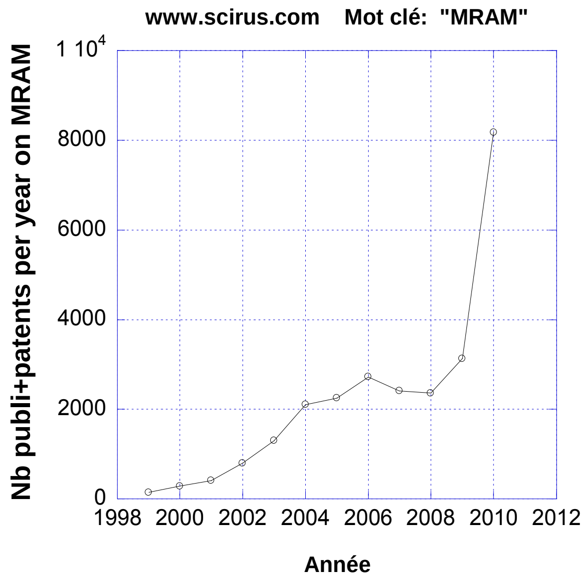
Spin current w/o charge current
Would allow full functionnality with
no heating / power dissipation !

Wei Kan et al (R. K. Kawakami's group), PRL 105, 167202 (2010).
B. Dlubak et al, (A. Fert's group) Appl. Phys. Lett. 97, 092502 (2010)



(FINAL) CONCLUSION

- Increasing interest for MRAM for stand-alone, embedded memories or "logic-in-memory"
- Spintronics brings non volatility to CMOS circuits for low-power, normally-off electronics
- Manufacturing technology mature enough with pure-play foundries entering the game
- Design environment "ready-to-use" as standard library tools
- Huge development potential



Important "cultural" gap between magnetics and microelectronics communities

→ Most MRAM players have HDD experience (e.g. magnetics "culture")

→ "Mutual education" mandatory to move towards adoption of spintronics in VLSI

Do not be afraid of magnetism and magnetic materials ! ☺